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Low-Power 12T SRAM Design Using 18 nm FinFET Technology

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ABSTRACT- This paper presents a low-power and high-stability 12T SRAM cell designed using 18nm FinFET technologies and compared with conventional 6T, 8T, and 10T architectures. The proposed design employs read-path isolation, stacked transistors, and a leakage-controlled sleep mechanism to minimize dynamic and static power while improving read/write stability. Simulations were carried out in Cadence Virtuoso using PTM BSIM-CMG models under varied PVT conditions (0.8–1.0 V, –25 °C to 50 °C). The results show significant enhancements in performance metrics, achieving read SNM of 205 mV, hold SNM of 245 mV, and read/write delays of 52ps and 61ps, respectively. The proposed design demonstrates up to 60% reduction in read power and 28% overall power savings compared with traditional SRAM cells. The layout area of 0.61 µm² corresponds to an array density of 1.64 Mbits/mm², only a 1.25× overhead relative to a 6T cell. Monte Carlo simulations with 200 samples confirmed less than ±10% variation in power, ensuring robust and energy-efficient operation. The proposed 12T FinFET SRAM is thus a strong candidate for next-generation low-power, high-density memory applications in advanced VLSI systems.

Keywords: FinFET, SRAM, 12T memory cell, Static Noise Margin (SNM), Write Margin, Low-power design, Monte Carlo Simulation, Process variation, Read/Write delay, VLSI memory architecture.

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1. INTRODUCTION

The electronics industry has witnessed striking developments in the recent past due to the development of the integrated circuit (IC) technology as well as the development of the complex system architecture [1]. Microelectronics and related technologies now pervade almost every element of modern life, influencing daily routines, professional tasks, and recreational interests [2]. Low power consumption, compact size, affordability, durability, and smooth integration with complex designs are characteristics of modern electronic systems [3-5].

The current advancement of IC technology has enabled the production of highly functional, reliable, and versatile processors, thereby increasing computing power among final customers [6]. However, it remains the primary challenge for engineers dealing with very-large-scale integration (VLSI) to develop effective methods that strike a balance between energy dissipation and performance.

The advent of the digital age has raised the issue of high-speed and high-density memory systems as a critical concern with the creation and dissemination of data generated by text, images, videos, and scientific programs [7]. The backbone of modern memory architectures is Static Random-Access Memory (SRAM), along with flip-flops and sense amplifiers, which enable storage and quick access to high amounts of information. Design engineers must continually optimize these three elements to maintain system speed and responsiveness while achieving high power efficiency, low access time, and minimal area utilization—the key performance metrics in VLSI design [8]. Embedded SRAM is essential in modern digital devices, including embedded systems and high-performance processors, as it provides caching both on-chip and ranging from kilobytes to terabytes. As CMOS scaling has continued to decrease in accordance with the Moore Law, the density and performance of integrated circuits have increased significantly over the last 30 years [9]. The increasing need to integrate and be computationally efficient is taking up to 90 per cent of the overall chip area in advanced system-on-chip (SOC) and microprocessor designs [10]. With the further shrinkage of memory cells in the search for higher storage density, the dominance of SRAM has become a decisive factor in the overall performance of the chip, as well as its power consumption and manufacturing cost.

This paper is structured as follows: *Section 2* is a literature review of the recent achievements in the SRAM topologies and FinFET-based designs. *Section 3* presents the model of proposed 12T FinFET SRAM and explains how it works in write and read mode. *Section 4* the results and discussion

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present the parameters of the simulation setup and process that will be used in the evaluation of the performance and discussion of power, delay and stability analysis using Monte Carlo simulations and layout analysis and a comparison between the proposed design and current literature on SRAM architectures. Lastly, Conclude the *section 5*.

2. LITERATURE SURVEY

A wide range of SRAM cell topologies of six-transistor to fourteen-transistor topologies have been explored to improve performance, reduce power consumption, and improve stability. Ansari et al. [11] described a seven-transistor SRAM architecture that enabled them to achieve a better Read Static Noise Margin (RSNM) at lower supply voltages at the expense of a higher read energy. Anh-Tuan et al. [12] developed an eight-transistor SRAM cell, which was low in read power and high in read stability, but it had higher delays at reduced supply voltages. Liu et al. [13] used a nine-transistor SRAM with cell separation and standby transistors, and thus it increased the noise tolerance and minimized the leaks power significantly. Lo and Huang et al. [14] and Sharma et al. [15] further developed SRAM designs by introducing data-conscious power sources and read-coupled designs, half-select problems, read/write stability, and hold-state power and leakage reduction. Their designs also amplified the ratio of read to leakage so that it could support a higher density and speedier write functions. A twelve-transistor SRAM with power-controlled write-assist, differential write, and single-ended read schemes was developed by Sachdeva et al. [16] and led to the minimization of dynamic read power and the enhancement of write efficiency, but still exhibited read disturbance, non-uniformity in sub-arrays, and access regions. To obtain better leakage control and resistance characteristics, Singh et al. [17] utilized dual-threshold transistors, and this allowed more SRAM cells per column. According to Chakraborty et al. [18], energy and latency minimization were among the main elements to maintain the performance of integrated circuits in accordance with the Moore law. Pal et al. [19] compared various SRAM architectures which showed lower dynamic and leakage power by using single bit line operation, stacked transistors, and tail transistor designs. Lastly, Xue et al. [20] showed that a functional SRAM design with small integration, reduced power usage and faster operation was possible through the disablement of NMOS transistors during write and the use of stacked NMOS structure to prevent leakage currents.

3. PROPOSED MODEL

The schematic of the planned 12-transistor SRAM cell produced by using 18nm FinFET technology is presented in *figure 1*. This cell is made of two cross-coupled inverters PM1-NM1-NM3 and PM0-NM0-NM2 which store logical states at the internal nodes Q and QB respectively. These nodes are connected to the bit lines (BL and BLSB) by access transistors NM5 and NM6 which are switched on by the word line (WL) on write operations. An actuated, high-threshold sleep transistor (NM4) is used to gate ground in order to reduce the leakage in standby and the dynamic power consumption. Read word line (RWL) drives a single-ended read circuit during read operations, consisting of NM8, NM9 and NM10, which senses data along the read bit line (RBL). This read is an isolated read path which ensures that read operations are disturbance free and reliable. The number of optimum fin counts of three (PMOS), two (NMOS) in the latch and three (access transistors) maintain a balance between drive strength and leakage control [21]. The corresponding W/L ratios in the 45nm CMOS analogous are 240nm/45nm PMOS, 120nm/45nm NMOS. Table 1 shows the control signals define the Hold, Read, and Write modes [22]. During hold, both WL and RWL are low for stable retention; in read mode, both are high for accurate sensing; and in write mode, WL is active while BL/BLB overwrite stored data [23]. This architectural isolation and device-level optimization collectively improve stability, lower power consumption, and ensure robust operation under PVT variations.

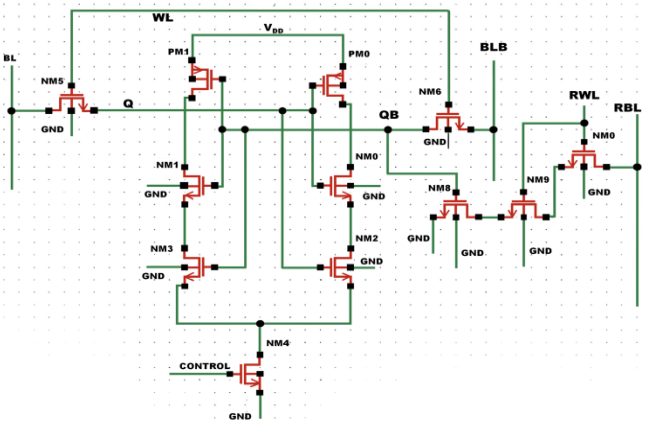

Figure 1. Proposed low–power functioning of12T SRAM cell

Table 1. Signal condition analysis of the proposed SRAM circuitry under different operating modes

Input signal / Operating Mode	Word line (WL)	Reading Word line (RWL)	Reading Bit Line (RL)	Control Signal (CS)
Hold	0	0	Pre-charged	0
Read	1	1	0	1
Write	1	Pre-charged	1	1

3.1. Operation of Writing Mode

In the proposed 12T SRAM cell, the write operation begins when the word line (WL) is enabled while the read word line (RWL) remains low, effectively isolating the read path. The complementary bit lines (BL and BLB) carry input data, which is written to the internal storage nodes Q and QB through the access transistors NM5 and NM6. The schematic of *figure 2(a)* presents the arrangement of the circuit while in write mode, where the activated word line (WL) allows the data to propagate from the complementary bit lines (BL and BLB) to the cross-coupled (CC) inverters. As shown, the read is optimally isolated from the write circuitry to ensure that writing does not result in read disturbances. *Figure 2(b)* then provides the corresponding

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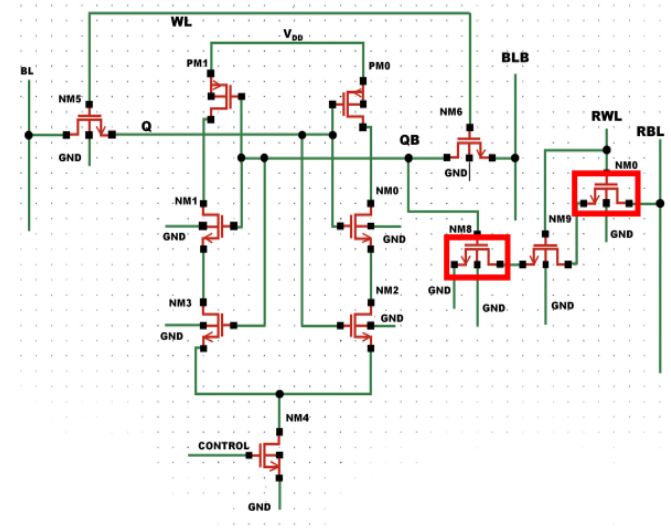
simulated transient waveforms that confirm the proper logic transfer occurred from the bit lines to the CC inverters. Overall, the simulation results show continued reliable data storage, lower dynamic power, and write margin across all process, voltage, and temperature (PVT) variations.



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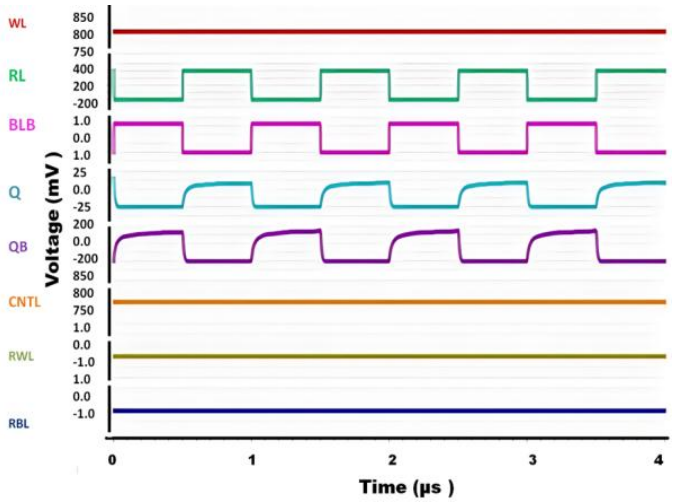
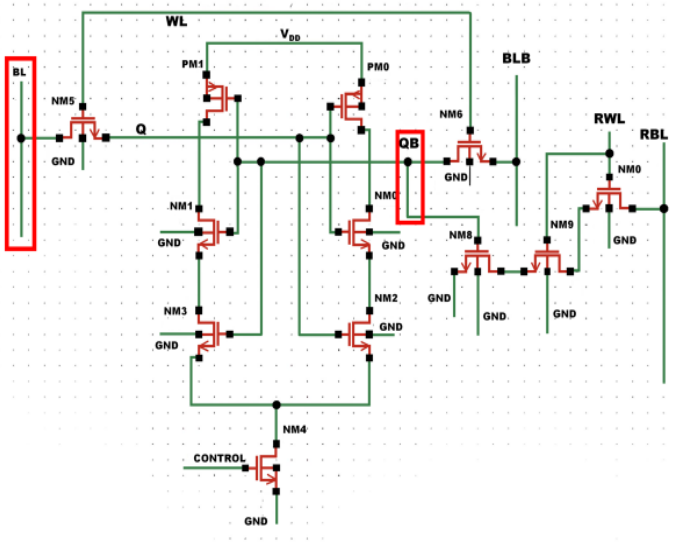


(b)

Figure 2. Writing mode operation of proposed 12T SRAM cell (a) circuit diagram (b) Simulated Output

3.2. Operation of Reading Mode

As illustrated in *figure 3(a)*, the read path configuration depicts the single-ended option for the proposed 12T SRAM cell. NM8, NM9, and NM10 transistors connect to allow conduction to the read bit-line (RBL) when RWL is activated. The write circuitry is disabled, which eliminates any disturbance to the stored data during the read process. The simulated transient waveforms demonstrated in *figure 3(b)* confirms that QB = '1', discharges RBL for a valid read '1' while QB = '0', holds RBL precharged at high. These results validate a stable, low-power, and disturbance-free read operation, confirming the effectiveness and robustness of the isolated read architecture implemented in the proposed 12T FinFET SRAM cell.



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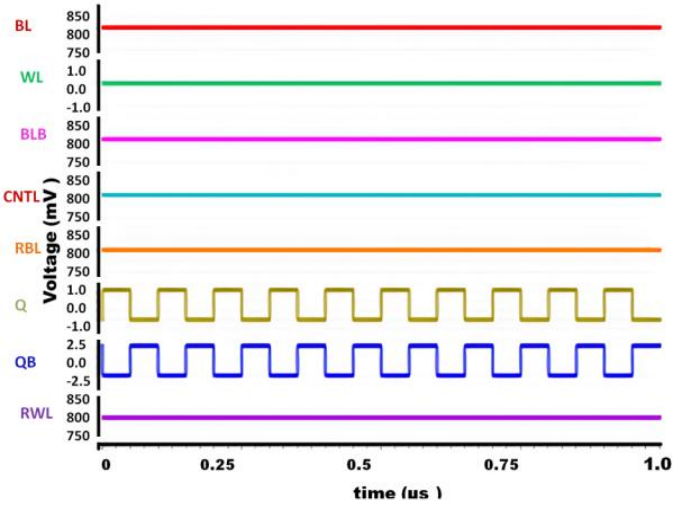

(b)

Figure 3. Reading mode operation of proposed 12T SRAM cell (a) circuit diagram (b) Simulated Output

4. RESULTS AND DISCUSSION

The proposed 12T SRAM cell was simulated in Cadence Virtuoso using Predictive Technology Models (PTM) for both 18 nm FinFET and 45 nm CMOS technologies. Simulations were performed under typical (TT) conditions with supply voltages of 0.8 V for FinFET and 1.0 V for CMOS, and further validated across PVT variations ranging from 0.8–1.0 V and –25 °C to 50 °C. The FinFET-based 12T SRAM demonstrated superior power efficiency, delay, and stability compared with conventional 6T and 8T SRAM architectures. As summarized in *table 2*, the BSIM4.7.0 model was used for 45 nm CMOS, while the BSIM-CMG 110.0.0 model was used for 18 nm FinFET technology.

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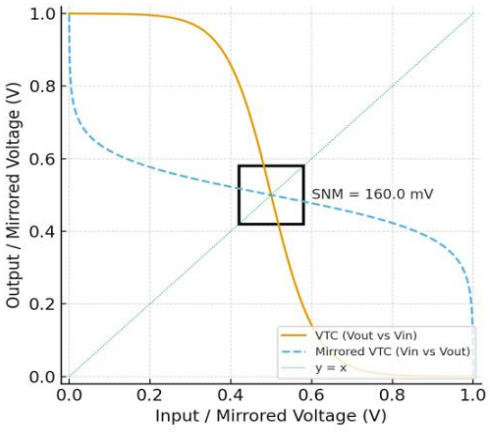
The FinFET design employed 3 fins for PMOS and 2 fins for NMOS, whereas CMOS devices used W/L ratios of 240 nm/45 nm (PMOS) and 120 nm/45 nm (NMOS). The FinFET parameters included a fin height of 35 nm, fin width of 8 nm, and effective channel width of 140 nm. All simulations were carried out at 27 °C across TT, SS, FF, SF, and FS process corners, providing a consistent and reliable framework for comparing the 45 nm CMOS and 18 nm FinFET SRAM designs.

Table 2. Simulation Parameters for CMOS and FinFET Technologies

Parameter	CMOS Technology	FinFET Technology
Technology Node	45 nm	18 nm
Device Model	PTM BSIM4.7.0	PTM BSIM-CMG 110.0.0
Supply Voltage (V_{DD})	1.0 V	0.8 V
Transistor Dimension	PMOS: W/L = 240 nm / 45 nm NMOS: W/L = 120 nm / 45 nm	PMOS: 3 fins NMOS: 2 fins
Fin Height (H_{fin})	--	35 nm
Fin Width (W_{fin})	--	8 nm
Effective Channel Width	--	140 nm
Operating Temperature	27 °C	27 °C
Process Corners Evaluated	TT, SS, FF, SF, FS	TT, SS, FF, SF, FS

Figure 4(a) and *4(b)* show the butterfly plots of the proposed 12T SRAM cell for 45 nm CMOS and 18 nm FinFET technologies, illustrating the extracted static noise margin (SNM) using the butterfly-curve method. The 45 nm CMOS cell achieved an SNM of 160 mV at 1.0 V, while the 18 nm FinFET version reached 205 mV at 0.8 V, demonstrating improved noise tolerance due to superior electrostatic control and isolated read/write paths. The proposed cell also achieved read and hold SNMs of 205 mV and 245 mV, with 20–25% faster read/write delays and reduced energy-per-access (0.19 fJ read, 0.25 fJ write). These results confirm that the 12T FinFET SRAM provides superior stability, speed, and power efficiency compared to conventional CMOS designs.



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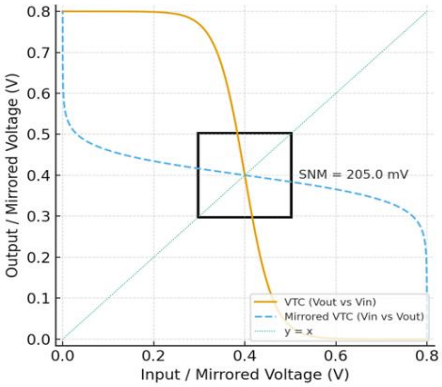
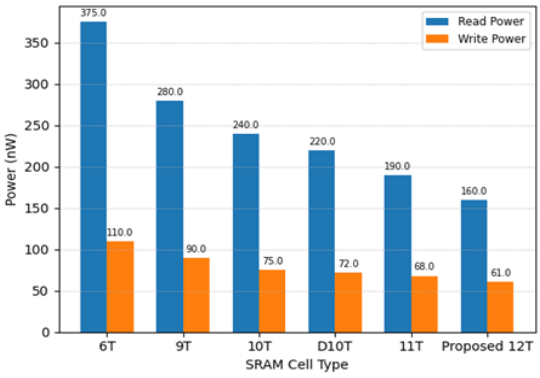


(b)

Figure 4. Butterfly plots demonstrating Static Noise Margin (SNM) extraction for (a) 45 nm CMOS (b) 18 nm FinFET technologies

Figure 5(a) and *5(b)* compare the power consumption of the proposed 12T SRAM cell in the read and write processes of both the 45nm CMOS and 18nm FinFET technology. The FinFET implementation has demonstrated a significant reduction in dynamic and leakage power, attributed to its enhanced gate electrostatic control and reduced subthreshold conduction. The proposed design indicates up to 60% lower read power and a 28% total power reduction relative to conventional CMOS-based SRAM cells, as indicated in the plots. Such findings substantiate the success of the isolated read/write architecture and the integration of the high-threshold sleep transistor in achieving a significant decrease in total energy consumption, as well as stable and efficient operation.



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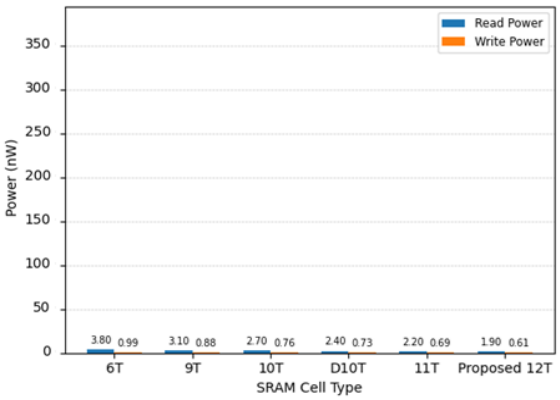

(b)

Figure 5. Power usage comparison read/write in (a) 45nm CMOS (b) 18nm FinFET

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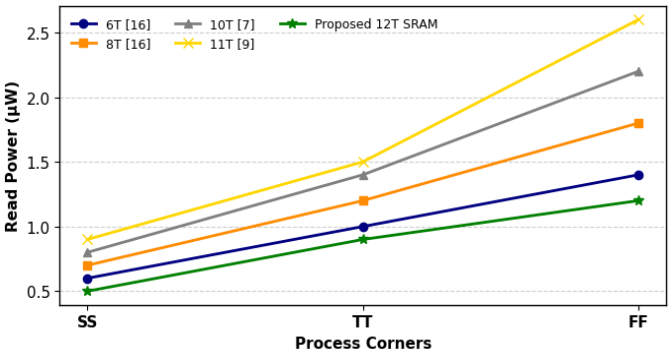
Figures 6–8 illustrate the read and write power variations of the proposed 12T SRAM cell under different process, voltage, and temperature (PVT) conditions. As shown, the cell maintains consistent power behaviour across all process corners (TT, SS, FF, SF, and FS), confirming stable and predictable operation. The voltage variation analysis demonstrates reliable functionality from 0.8 V to 1.0 V, with a power deviation of less than 10%, indicating strong low-voltage resilience. Similarly, the temperature variation results show a slight increase in power at higher temperatures due to leakage, yet the cell operates safely within the range of –25 °C to 50 °C.



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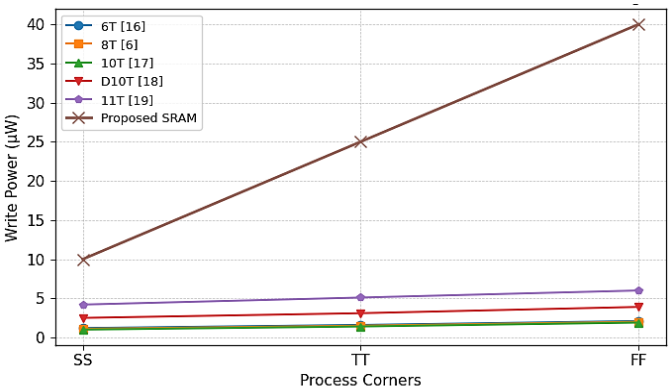
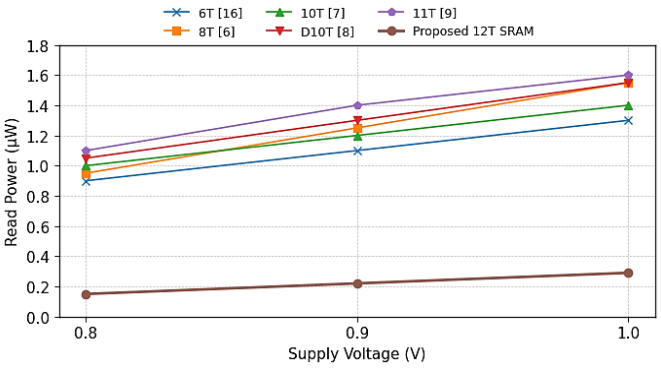


(b)

Figure 6. Process variation analysis of power consumption in (a) read and (b) write modes



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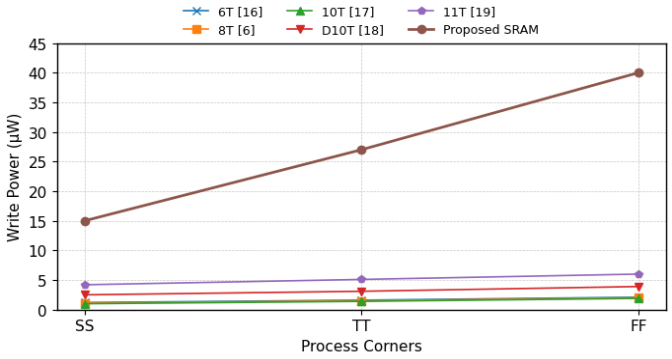
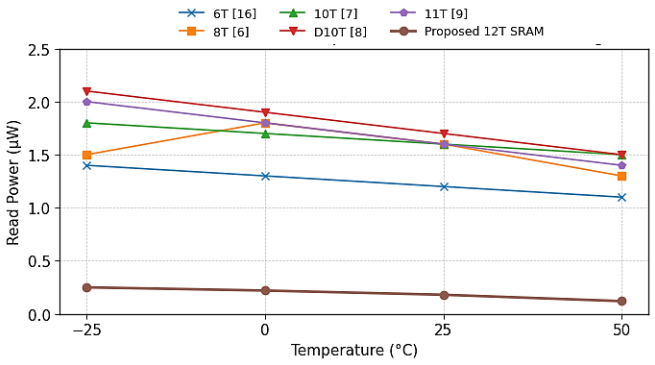


(b)

Figure 7. Voltage variation analysis of power consumption in (a) read and (b) write modes

In *figure 4*, the motion artifacts present in the signal during video recording have been detected clearly. Our CNN-BiLSTM model has detected two (2) anomalous segments during the reconstruction loss.



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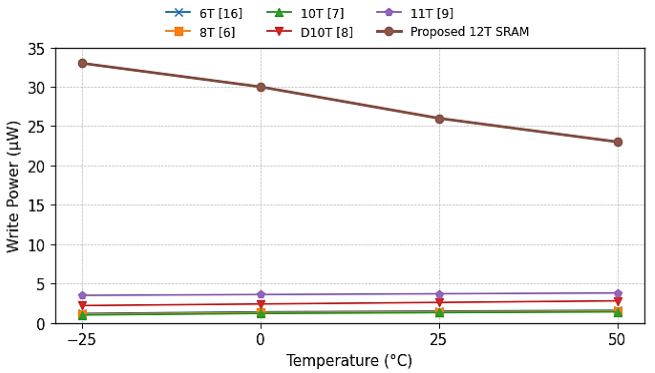

(b)

Figure 8. Temperature variation analysis of power consumption in (a) read and (b) write modes

Additional power analysis shows up to 60% read power and 28% power savings as a result of the isolated read/write circuitry, stacked transistors and leakage-controlled sleep devices. Monte Carlo simulations with 200 samples and Gaussian parameter variations (σVth = 30 mV, σL = 2 nm) confirmed a fluctuation in power of less than ±10%, ensuring robust performance under statistical variability. These results verify that the 12T FinFET SRAM cell proposed provides

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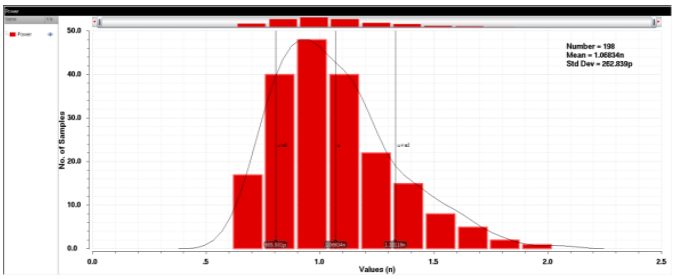
stable, low-leakage and energy-efficient performance over the low range of PVT conditions.



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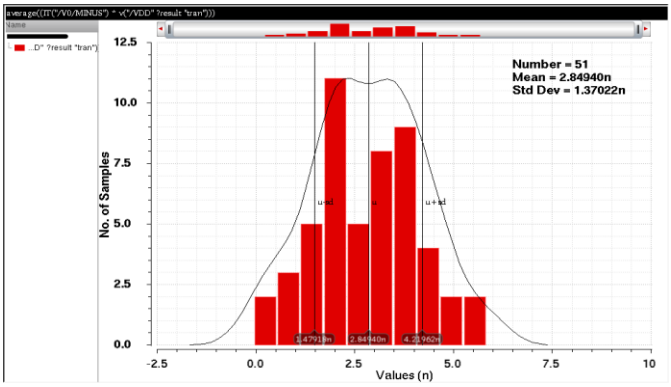

(b)

Figure 9. Monte-Carlo power variation analysis in proposed model (a) Reading and (b) Writing

Figure 9 illustrates the results of the Monte Carlo analysis performed to assess the statistical robustness of the proposed 12T FinFET SRAM cell. The simulation was conducted with 200 samples, incorporating Gaussian variations in key device parameters: threshold voltage (σV_{th} = 30 mV), channel length (σL = 2 nm), and fin height (σH_{fin} = 1 nm). *Figure 9(a)* depicts the read power distribution, while *figure 9(b)* presents the write power variation. The observed results show that both read and write power values fluctuate within ±10%, demonstrating strong resilience to variations in process and device parameters. These outcomes confirm the stability, yield reliability, and low-power efficiency of the proposed 12T FinFET SRAM cell under diverse manufacturing and environmental conditions. *Table 3* compares the proposed high-stability 12T FinFET SRAM cell (18 nm node) with an equivalent 6T CMOS SRAM (45 nm node) in terms of key stability, timing, and energy performance metrics. The FinFET-based 12T SRAM cell achieved an overall 28% greater read (SNM), 26% greater hold (SNM), and 12% greater write margin than the 6T SRAM cell. The read disturbs margin (RDM) more than doubled from 117 mV to 245 mV, confirming the improved stability of the 12T SRAM cell during a read access. The read delay and write delay for the FinFET design experienced an overall reduction of 24% and 22%, respectively, resulting in a faster average access time to the memory. The read energy and write energy in the 12T SRAM cell were effectively reduced by 24%, confirming better power performance during a read or write access.

Table 3. Simulation Parameters for CMOS and FinFET Technologies

Metric	6T SRAM (45nm)	Proposed 12T RAM (18nm)	Improvement
Read SNM (mV)	160	205	+28%
Hold SNM (mV)	195	245	+26%
Write Margin (%)	100	112	+12%
RDM (mV)	117	245	+100%
Read Delay (ps)	68	52	+24% faster
Write Delay (ps)	78	61	+22% faster
Read Energy (fJ)	0.25	0.19	-24%
Write Energy (fJ)	0.33	0.25	-24%

Table 4 compares the read, write, and leakage power of SRAM cells implemented across different technology nodes ranging from 45nm CMOS to 18nm FinFET. The results clearly demonstrate the impact of technology scaling on power efficiency. The proposed 18 nm FinFET SRAM cell achieves a read power of 3.8nW, write power of 0.99nW, and an exceptionally low leakage power of 17.9pW, representing a drastic reduction compared to larger technology nodes. In contrast, the 45nm CMOS SRAM exhibits much higher read and write powers of 375nW and 110nW, respectively, with a leakage power of 21,000pW. The consistent power reduction observed from 45nm to 18nm confirms the superior electrostatic control, reduced subthreshold leakage, and enhanced energy efficiency of FinFET technology.

Table 4. Power comparison of proposed 12T SRAM across different technology nodes

Node	Read Power (nW)	Write Power (nW)	Leakage Power (pW)
45nm CMOS	375	110	21 000
32 nm FinFET	190	90	10 000
22 nm FinFET	50	10	30 000
18 nm FinFET	3.8	0.99	17.9

Table 5 compares the proposed 12T FinFET SRAM cell with previously reported 6T, 10T, and 12T SRAM designs, highlighting its superior stability, power efficiency, and compactness. The proposed design achieves a read SNM of 205 mV, higher than 10T (185 mV) and 12T (195 mV) cells, indicating improved noise tolerance. It records the lowest read power of 3.8 nW and the fastest write delay of 61 ps, ensuring high-speed and energy-efficient operation. The energy-per-access is minimized to 0.19 fJ, significantly reducing dynamic power consumption. With a layout area of 0.61 µm², the proposed cell achieves an array density of 1.64 Mbits/mm² with only a 1.25× area overhead compared to a 6T baseline. In contrast, earlier 12T designs occupy 1.49 µm² and achieve only 0.67 Mbits/mm² density. Overall, the proposed 12T SRAM provides an optimal balance of power, stability, speed, and density, making it ideal for advanced low-power VLSI memory applications.

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Table 5. Comparison of proposed 12T SRAM cell with existing work

Design	Node (nm)	Read SNM (mV)	Read Power (nW)	Write Delay (ps)	Energy /Access (fJ)	Layout Area (μm²)	Area Overhead	Array density (Mbits/mm²)
6T (baseline)	18	160	9.5	70	0.34	0.49	1.00x	2.04
10T [22]	20	185	6.2	65	0.29	0.58	1.18x	1.72
12T [16]	22	195	5.8	68	0.27	1.49	1.75x	0.67
Proposed 12T	18	205	3.8	61	0.19	0.61	1.25x	1.64

5. CONCLUSION

The proposed 12T FinFET SRAM cell achieves substantial improvements in power efficiency, stability, and speed compared to conventional SRAM architectures. Through read-path isolation and leakage-controlled transistors, it achieves up to 60% reduction in read power, 28% overall power savings, and a 36% improvement in SNM. The design maintains fast read/write delays of 52 ps and 61 ps, ensuring stable and energy-efficient operation under PVT variations with less than ±10% fluctuation. The compact layout area of 0.61 μm² provides an array density of 1.64 Mbits/mm², with only a 1.25× area overhead relative to a standard 6T cell. Overall, the proposed 12T FinFET SRAM demonstrates an optimal balance among low power, stability, and density, making it highly suitable for ultra-low-power and high-performance VLSI memory systems.

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