FOREX Publication
Open Access | Rapid and quality publishing

International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

Fixed Frequency SVPWM+PI Controlled LCL Shunt Active Power Filter in *dq* Frame for Microgrids

Dr. Mehul Dansinh Solanki[1*], Dr. Ashokkumar Parmar[2], Dr. Jaydeepsinh Sarvaiya[3], S. K. Joshi[4], Dr. Mayur V. Gojiya[5]

[1]*Assistant Professor in Electrical Engineering, Shantilal Shah Engineering College, Bhavnagar affiliated to Gujarat Technological University, Gujarat, India; Email: mdsolanki@elec.ssgec.ac.in*

[2]*Associate Professor in Electrical Engineering, Shantilal Shah Engineering College, Bhavnagar affiliated to Gujarat Technological University, Gujarat, India; Email: abparmar80@gmail.com*

[3]*Assistant Professor in Electrical Engineering, Shantilal Shah Engineering College, Bhavnagar affiliated to Gujarat Technological University, Gujarat, India; Email: Jbs201182@gmail.com*

[4]*Retired Professor and Head of Electrical Engineering, Faculty of Technology and Engineering, The Maharaja Sayajirao University of Baroda, Vadodara, Gujarat, India; Email: skjoshi@ieee.org*

[5]*Assistant Professor in Electrical Engineering, Shantilal Shah Engineering College, Bhavnagar affiliated to Gujarat Technological University, Gujarat, India; Email: mayur.gojiya010@gmail.com*

***Correspondence:** *Dr. Mehul Solanki, Email: mdsolanki@elec.ssgec.ac.in*

ABSTRACT- This paper presents the design of simple, robust, and efficient shunt active power filter (SAPF) using a loop in loop (cascaded) PI controller and Space vector pulse width modulated synchronous reference frame (*dq*) controller to mitigate harmonics from a three-phase diode rectifier (nonlinear load) catering to variety of loads (R, and R-L), supplied by a microgrid (week grid) having plethora of distributed generator, exhibiting heuristic nature. The intermittent nature of DGs leads to variation in voltage and frequency, and load variation aggravates this situation further. Placement and availability of DGs in the microgrid lead to the variation in cable length, causing variation in the reactance presented between the source and the point of common coupling, where a SAPF is deployed. A robust control mechanism of SAPF has been presented here that gives compliance to IEEE-519 amidst the mentioned perturbations in voltage, frequency, and grid reactance using a passively damped LCL filter and a smaller DC-bus capacitor due to the presence of SVPWM control. A constant frequency switched Space Vector Pulse Width Modulation (SVPWM) control makes the SAPF simpler and more reliable. Further, a cascaded PI controller, one controlling DC-bus voltage and another controlling the filter's current, makes it more efficient and reliable. Simulation and comparative analytical results of SVPWM with that of Sinusoidal PWM (SPWM) validate the design's suitability for enhancing power quality in the given system.

Keywords: Cascaded PI control, LCL filter, Microgrid, SAPF, SVPWM control.

ARTICLE INFORMATION

Author(s): Dr. Mehul Dansinh Solanki, Dr. Ashokkumar Parmar, Dr. Jaydeepsinh Sarvaiya, S. K. Joshi, and Dr. Mayur V. Gojiya;
Received: 04/10/2025; **Accepted:** 15/12/2025; **Published:** 30/12/2025;
E- ISSN: 2347-470X;
Paper Id: IJEER 0410A04;
Citation: 10.37391/ijeer.130433
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-13/ijeer-130433.html

Publisher's Note: FOREX Publication stays neutral with regard to jurisdictional claims in Published maps and institutional affiliations.

1. INTRODUCTION

Power quality improvement in electrical systems is crucial due to the growing presence of nonlinear loads, which introduce harmonic distortion and negatively impact grid stability, as well as exacerbate power losses. The SAPF serves as an effective solution for harmonic mitigation and reactive power compensation. SAPFs are replacing the conventional passive filter due to their enormous advantages. SAPF is a harmonic generator that injects harmonics having a magnitude equal to that of a particular harmonic at PCC with a phase delayed by 180°.

The efficacy of a SAPF hinges on the accuracy of reference/compensating current for harmonics and reactive power compensation, and it drives a three-phase voltage source converter (SAPF). Nonlinear loads, renewable integration, and grid code requirements have propelled the advancements in SAPF control, resulting in a wide range of methodologies that combine classical, modern, adaptive, and optimization-based controllers.

Classical PI and PR controllers are the most popular choices for the control of SAPF, but prove inefficient and non-robust with parametric variation [0]. The deadbeat/hysteresis current controller's [0] variable switching frequency degrades the robustness of PI/PR controllers. Modern control techniques such as Model Predictive Control (MPC) [0], repetitive control [0],

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

and sliding-mode control [0] offer fast dynamic response at the cost of complicated controller design, and hence lack simplicity and cost effectiveness. Fuzzy Control [0] requires complex design and tuning, and can suffer from chattering or instability. Furthermore, the performance of the Optimal Neural network-based controllers [0] relies on the quality of the training data and may increase real-time computational and memory requirements. Typically, they perform offline, requiring re-tuning under system changes, which can be limited by convergence and cost-function definition, and are less suited for highly dynamic systems. Instantaneous Reactive Power (p–q) Theory-based control inherently assumes an ideal voltage source, which is seldom the case with a weak grid having a high *X/R* ratio (microgrid), and can exhibit compensation delays [0]. This work addresses limitations in the existing SAPF literature, where L or LC filters are commonly used with VSCs, resulting in larger component sizes, higher costs, increased losses, resonance issues, and sensitivity to grid impedance that compromise stability and harmonic compensation speed [0]. In contrast, the proposed approach employs an LCL filter for superior switching frequency harmonic attenuation [0], simple yet efficient passive damping [0], faster dynamic response, and enhanced robustness to source impedance variations [0][0], complemented by simple yet efficient and less computationally involving fixed frequency SVPWM for higher DC-link utilization [0] which is mimicking sinusoidal PWM (SPWM). Adaption of SVPWM reduces harmonics, fixed frequency switching relieves controller form the burdosom task of sector identification and timing calculation, and improves efficiency due to higher DC-link utilization over traditional SPWM technique. This cascaded PI + SVPWM + LCL strategy, further integrated with electrically enhanced Phase Locked Loop structure (ePLL) [0] for microgrid conditions featuring combined voltage, frequency, and harmonic perturbations, establishes the novelty and superior performance.

The remainder of this paper is organized as follows: *Section 2* describes the system configuration and modeling of the proposed SAPF. *Section 3* presents the design of SAPF, *section 4* introduces the control strategy, including cascaded PI, SVPWM, LCL filter design, and ePLL integration. *Section 5 and 6* discusses simulation setup and comparative results, validating the proposed approach. *Section 7* discussed about the requirements of real time implementation, and section 8 concludes the paper with key findings and future research directions.

2. SHUNT ACTIVE POWER FILTER AND ITS MATHEMATICAL MODEL

The mathematical model of a three-phase SAPF with an LCL filter describes the dynamics of the AC-side and the DC-link of SAPF. The model assumes a VSC connected to the grid at the PCC through the LCL filter, with passive damping (resistor R_d) in series with the filter capacitor (C_f). The system of SAPF shown in *fig.1* is considered balanced, and parasitic resistances are neglected for simplicity. The model is presented per phase (*abc* frame) and can be transformed to *dq* frame for control purposes.

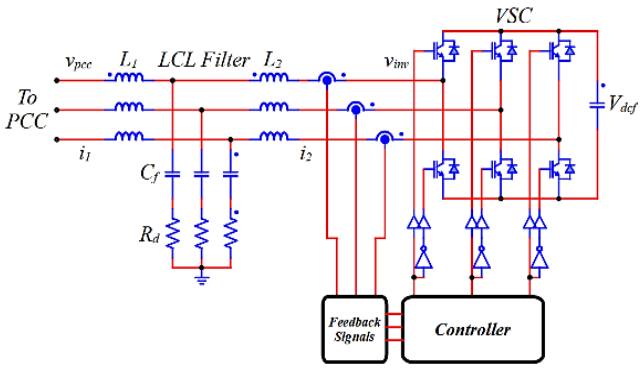

Figure 1. Block Diagram of SAPF

2.1. AC side model

The AC side of the SAPF is dominated by LCL filter. Its dynamics with series damping, are governed by Kirchhoff's laws. Here, the junction voltage is given by

$$v_j = v_{cf} + R_d i_c = v_{cf} + R_d(i_1 - i_2) \tag{1}$$

Converter-side inductor:

$$L_1 \frac{di_1}{dt} = v_{inv} - v_j = v_{inv} - v_{cf} - R_d(i_1 - i_2) \tag{2}$$

Grid-side inductor:

$$L_2 \frac{di_2}{dt} = v_j - v_{pcc} = v_{cf} + R_d(i_1 - i_2) - v_{pcc} \tag{3}$$

Filter capacitor:

$$C_f \frac{dv_{cf}}{dt} = i_c = i_1 - i_2 \tag{4}$$

These are coupled first-order differential equations for states (i_1, i_2, v_{cf}). These equations lead to a state-space model,

$$\dot{x} = \mathrm{A}x + \mathrm{B}u$$
$$\mathrm{y} = \mathrm{C}x \tag{5}$$

Where,
$x = [i_1\ i_2\ v_{cf}]^T$, $u = [v_{inv}\ v_{pcc}]^T$, $y = i_2$, and

$$A = \begin{bmatrix} \frac{-R_d}{L_1} & \frac{R_d}{L_1} & \frac{-1}{L_1} \\ \frac{R_d}{L_2} & \frac{-R_d}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & \frac{-1}{C_f} & 0 \end{bmatrix}, B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{-1}{L_2} \\ 0 & 0 \end{bmatrix} \text{ and } C = [0\ 1\ 0]$$

2.2. DC Side Model

From the power balance formulation,

$$C_{dc} \frac{dv_{dc}}{dt} = i_{dc} - \frac{v_{dc}}{R_{loss}} \tag{6}$$

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

where i_{dc} is the average inverter current, approximated in *dq* frame as:

$$i_{dc} = \frac{3}{2v_{dc}}\left(v_{inv,d}i_{1,d} + v_{inv,q}i_{1,q}\right) \quad (7)$$

This mathematical model has been used to derive the controller for a SAPF.

Table 1. AC Source Parameters

Parameter	Symbol	Value	Unit
Line-to-Line Voltage (RMS)	V_{LL}	415±20%	V
Grid Frequency	f	48, 50, 52	Hz
Source Inductance (per phase)	L_s	350, 700	µH

3. DESIGN OF APF PARAMETER

3.1. LC Filter for the Rectifier

The LC filter is placed on the DC side of the three-phase full-bridge diode rectifier to reduce ripple in the output voltage (<5%) and current (<10%). The dominant ripple frequency for a three-phase rectifier is the 6th harmonic (300Hz) of the supply frequency.

The inductor limits the current ripple by providing impedance to the 300 Hz ripple voltage.

$$L_{dc} \geq \frac{V_{ripple,6}}{\Delta I_{dc} \cdot 2\pi f_{ripple}} \approx \frac{15.9}{12.55 \times 2\pi \times 300} \approx 0.00671\,H \quad (8)$$

Consider a standard 7.5mH as L_{dc}.

The capacitor (C_{dc}) filters the ripple current to maintain low voltage ripple across the load. It has been designed using the resonant frequency of 48Hz,

$$C_{dc} = \frac{1}{(2\pi f_{res})^2 L_{dc}} = \frac{1}{(2\pi * 48)^2 \times 7.5 \times 10^{-3}} \approx 1350\mu F \quad (9)$$

Consider a standard 1500µF as C_{dc}.

Table 2. Rectifier and Load Parameters

Parameter	Symbol	Value	Unit
DC Load	R_{dc}	2.23, 1.115	Ω
DC Filter Inductance	L_{dc}	7.5	mH
DC Filter Capacitance	C_{dc}	1500	µF

3.2. DC-link capacitor of SAPF

C_{dcf} limits voltage ripple to 3% (kv,max = 0.03, ΔVrms ≈ 21 V) from n=6f (300 Hz) fluctuations due to harmonic compensation.

$$C_{dcf} \geq \frac{I_{cn,rms}}{nk_{v,max}V_{dc}2\pi f} = \frac{44}{6 \times 0.03 \times 700 \times 314} \approx 1{,}112\,\mu F \quad (10)$$

Consider a standard 1500µF as C_{dcf}.

3.3. LCL filter

The LCL filter (L_1, C_f, L_2, and R_d) attenuates switching harmonics (>40 dB at f_{sw}) while ensuring fast dynamics. The source inductance L_s adds to L_2, forming effective grid-side inductance $L_g = L_2 + L_s$.

Furthermore, these parameters are designed with constraints as,

- Total inductance $L_1 + L_g < 0.3$ pu
- $C_f < 0.05$ pu (limit reactive power)
- Resonant frequency: 500 Hz < f_{res} < 10 kHz (10f to 0.5 f_{sw})
- Attenuation at $f_{sw} \geq 40$ dB
- Damping factor $\zeta \approx 0.1–0.2$

Converter-Side Inductor (L_1):

$$L_1 = \frac{V_{dc}}{4f_{sw}\Delta I_{pp}} = \frac{700}{4 \times 20000 \times 17} \approx 0.515\,\text{mH} \quad (11)$$

Select L_1 = 0.5 mH. Voltage drops at 50 Hz: ≈ 1.13 V (<1% Vph).

Filter Capacitor (C_f):
$Limit: C_f \leq 0.05C_b \approx 130\mu F. Select\ C_f = 10\mu F.$
$Reactive\ power: Q_{C_f} \approx 540W (< 0.4\%P_b).$

Grid-Side Inductor (L_2):
Set $L_2 \approx L_1$ for symmetry. Select L_2 = 0.5 mH.
Effective $L_g = L_2 + L_s$ = 0.5 + 0.2 = 0.7 mH.

Resonant Frequency:

$$f_{res} = \frac{1}{2\pi\sqrt{\frac{L_1 L_g}{L_1 + L_g}C_f}} \approx \frac{1}{2\pi\sqrt{\frac{0.5 \times 0.7 \times 10^{-3}}{0.5 + 0.7} \times 10 \times 10^{-6}}} \approx 2{,}760\,\text{Hz} \quad (12)$$

Within 500 Hz–10 kHz.

Damping Resistor (R_d):

$$R_d \approx \frac{1}{3 \times 2\pi f_{res} C_f} \approx \frac{1}{3 \times 2\pi \times 2{,}760 \times 10 \times 10^{-6}} \approx 1.92\,\Omega \quad (13)$$

$Select\ R_d = 2\Omega.$

Attenuation at f_{sw}:

$$|H(f_{sw})| \approx \frac{1}{(2\pi f_{sw})^2 L_1 C_f L_g} \approx 0.0032 \quad (14)$$

Attenuation ≈ 1/0.0032 ≈ 312

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

Table 3. SAPF Parameters

Parameter	Symbol	Value	Unit
DC-Link Voltage	V_{dcf}	700	V
Switching Frequency	f_{sw}	20	kHz
Grid's Frequency	f	48 to 52	Hz
Converter-Side Inductance	L_1	0.5	mH
Filter Capacitance	C_f	10	µF
Grid-Side Inductance	L_2	0.3	mH
Effective Grid Inductance	L_g	0.3 to 1.0	mH
Damping Resistor	R_d	2	Ω
Resonant Frequency	f_{res}	2760	Hz
DC-Link Capacitance	C_{dcf}	1500	µF
Permissible Ripple Factor		3	%

4. CONTROL IN THE SYNCHRONOUS (*dq*) FRAME OF REFERENCE

Park Transformation [0] converts *3-ϕ* currents (i_a, i_b, i_c) into *2-ϕ* currents (i_d, i_q), which are synchronously rotating at ωt (=θ). Here is derived from the voltage at PCC through ePLL. In *dq* frame, the fundamental components look like DC, and its multiples\harmonics look like ripples.

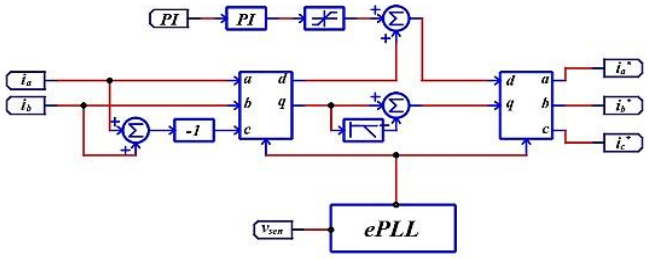

Figure 2. Reference Current Calculator

A constant and ripple-free DC bus is anticipated for the precise control, and hence a PI controller, regulating the voltage at the DC bus. This error is added to i_d as shown in *fig. 3*.

To separate the harmonic component associated with i_q it is filtered through a HPF [0] (realized through a LPF [0][0]).

These two signals make the input of the inverse park transformation block [0], which is driving the switching signal generator.

4.1. Switching Signal Generator

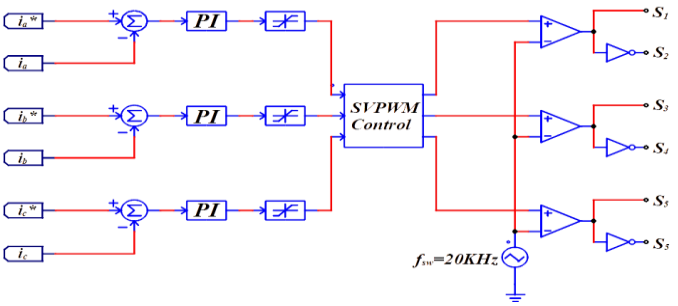

Figure 3a: SVPWM Switching Signal Generator

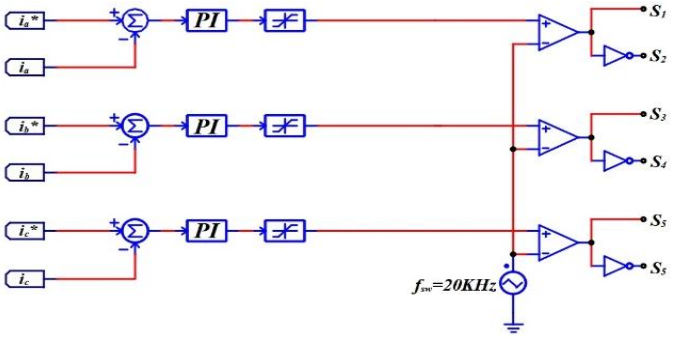

Figure 3b. SPWMS witching Signal Generator

The three currents generated by Prak's transformation block (i_{dq}-i_{abc}) work as a reference (i_{abc}*) and the same is compared with the output of the VSC acting as a SAPF. The output of the same is driving the PI controller and is being limited by a limiter in a tight band of 1V, as shown in *fig.4*. The output of the same is driving a constant frequency SVPWM controller.

4.2. Fixed frequency space vector pulse width modulator

It has been opted to drive the switches through fixed frequency SVPWM due to their superior DC-bus (15% higher) utilization and better compliance with switching frequency harmonics over the SPWM, and at the same time, it is simpler to implement, as it is relieved from the burden of timing and sector identification [0].

4.3. Design of a cascaded controller

The outer voltage loop controller can be designed using its dynamic model, and the same can be presented in the form of a transfer function as,

$$G_v(s) = \frac{V_{dc}}{i_d} = \frac{3V_{ph}}{C_{dc}V_{dc}s} = \frac{3 \times 239.6}{1500 \times 10^{-6} \times 700 \times s} \approx \frac{683.7}{s} \quad (15)$$

Cascaded with the transfer function of a PI controller results into,

$$T_v(s) = \frac{G_{PI,v}(s)G_v(s)}{1 + G_{PI,v}(s)G_v(s)} = \frac{\left(K_{p,v}s + K_{i,v}\right) \cdot 683.7/s}{1 + \left(K_{p,v}s + K_{i,v}\right) \cdot 683.7/s} = \frac{683.7K_{p,v}s + 683.7K_{i,v}}{s^2 + 683.7K_{p,v}s + 683.7K_{i,v}} \quad (16)$$

A PI controller can be designed by judiciously considering the design goals and which are,

Desired bandwidth (BW): ~10–20 Hz (slow to avoid interfering with current loop, ~100–200 times slower than f_{sw}/100).

Phase margin: ~60° for stability.

Approximated as a second-order system with natural frequency $\omega_n (= 2\pi \times 15\, rad/s)\ for\ BW\ of$ 15Hz, and damping ratio ζ = 0.707 (for optimal damping), leads to,

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

$$\omega_n = \sqrt{683.7K_{i,v}}, \quad 2\zeta\omega_n = 683.7K_{p,v} \tag{17}$$

$$K_{i,v} = \frac{\omega_n^2}{683.7} \approx \frac{94.2^2}{683.7} \approx 13.0 \tag{18}$$

$$K_{p,v} = \frac{2\zeta\omega_n}{683.7} \approx \frac{2 \times 0.707 \times 94.2}{683.7} \approx 2.0 \tag{19}$$

The faster inner current control loop can similarly be designed by approximating the dominant inductance ($L_1 + L_g$ = 1.2 mH) below f_{res} (2,760 Hz), and considering current control bandwidth <1 kHz for the plant,

$$G_i(s) = \frac{i_1(s)}{v_{inv}(s)} \approx \frac{1}{(L_1 + L_g)s} = \frac{1}{1.2 \times 10^{-3}s} \approx \frac{833.3}{s} \tag{20}$$

The closed-loop transfer function,

$$T_i(s) = \frac{833.3K_{p,i}s + 833.3K_{i,i}}{s^2 + 833.3K_{p,i}s + 833.3K_{i,i}} \tag{21}$$

Considering BW: ~1–2 kHz (to track harmonics up to 1250 Hz, <f_{sw}/10), and phase margin: ~60°, the controller can be designed as,

$$K_{i,i} = \frac{\omega_n^2}{833.3} \approx \frac{9{,}425^2}{833.3} \approx 106{,}600 \tag{22}$$

$$K_{p,i} = \frac{2\zeta\omega_n}{833.3} \approx \frac{2 \times 0.707 \times 9{,}425}{833.3} \approx 16.0 \tag{23}$$

Table 4. Parameters of cascaded PI Controller

Parameter	Symbol	Value	Unit
Voltage Loop Proportional Gain	K_{pv}	0.2	-
Voltage Loop Integral Gain	K_{iv}	13	s^{-1}
Current Loop Proportional Gain	K_{pi}	16	-
Current Loop Integral Gain	K_{ii}	106600	s^{-1}

4.4. Stability Analysis of the Designed Cascaded Controller

The stability assessment of the designed inner current loop controller was conducted using Bode plot analysis of SAPF under the proposed control, complemented by impedance-based evaluation of the cascaded LCL filter and grid impedance.

4.4.1. Bode Plot

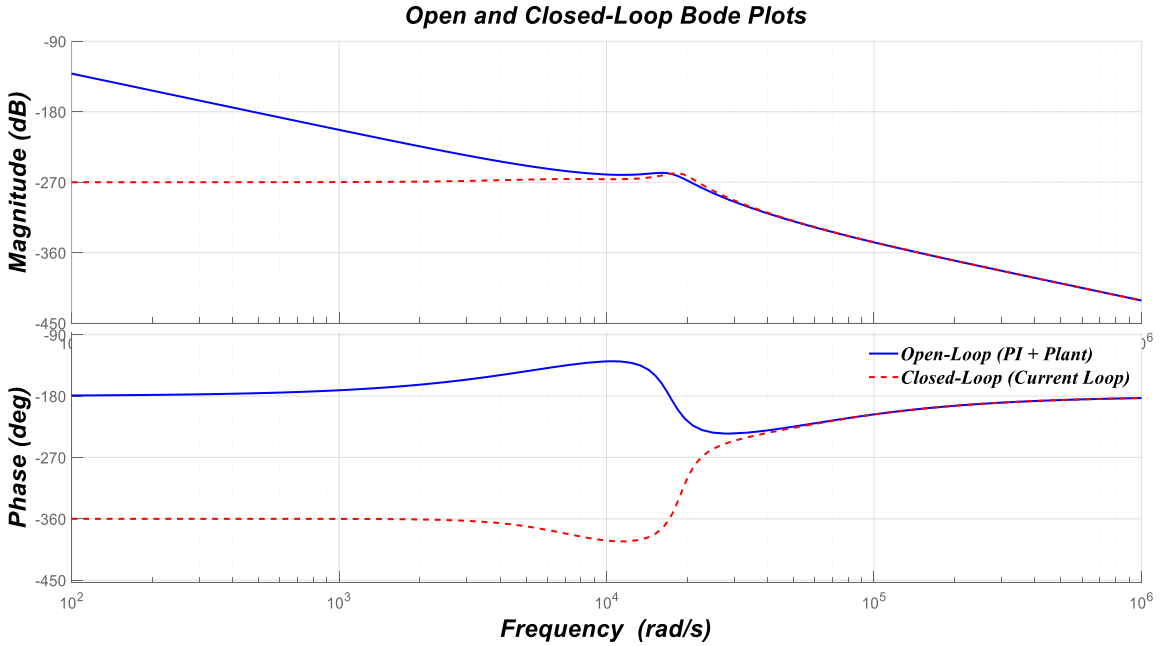

Figure 4. Bode Plot of Open and Closed Loop SAPF

The Bode plot shown in *fig. 4* indicates a stable, well-tuned current loop. The open-loop magnitude crosses 0 dB around 10^4 rad/s, and the corresponding phase remains comfortably above −180°, suggesting an adequate phase margin (>45°). The closed-loop curve shows limited peaking near bandwidth and a clean roll-off, implying good damping of the LCL resonance and minimal sensitivity to grid variations. The convergence of

open and closed-loop responses past the crossover, alongside the absence of multiple crossovers or sharp phase dips, supports robust stability. Overall, the PI-shaped loop achieves bandwidth safely below the resonant features, balancing responsiveness with resilience.

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

4.4.2. Impedance Plot

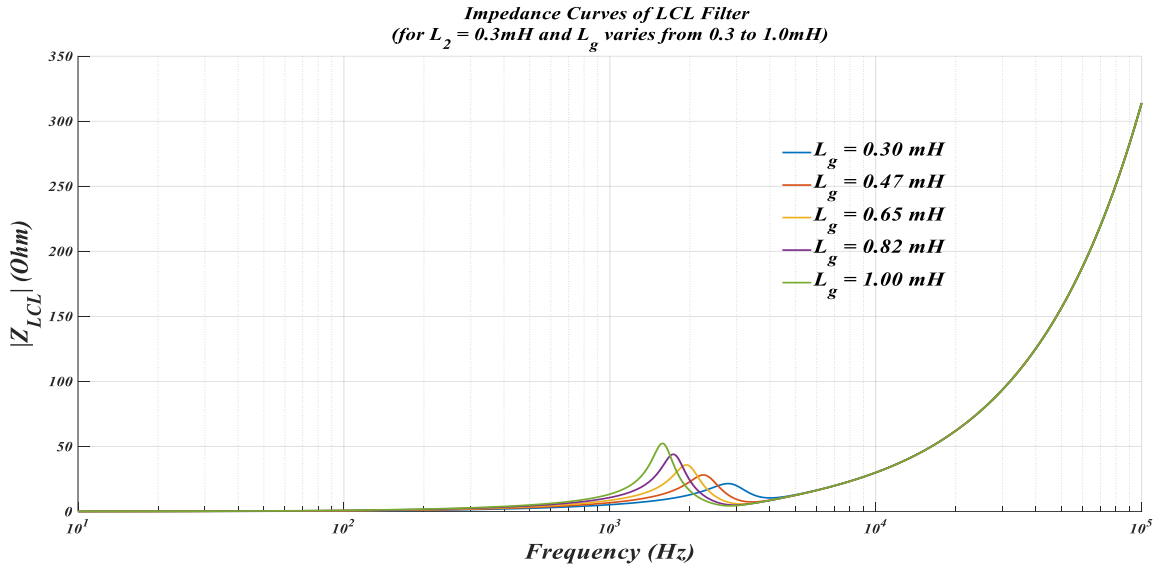

Figure 5. Impedance Plot of LCL filter with variable Grid Impedance

The impedance plot of *fig.5* demonstrates a well-controlled LCL resonance that shifts to lower frequencies as L_g increases (0.30 – 1.00 mH), effectively shaping the filter away from typical switching bands. The rounded resonance profiles under passive damping (R_d=2 Ω) confirm stable current-loop operation and mitigate oscillatory risks even with L_g variations up to 1.0 mH. Robustness is further indicated by the absence of sharp spikes and consistent high-frequency attenuation (resonance occurs between 1567 Hz to 2762 Hz with amplitude variation of 21.4 Ω to 52.4 Ω), ensuring tolerance to source impedance changes without destabilizing interactions.

5. PERFORMANCE EVALUATION OF SAPF IN *dq* FRAME

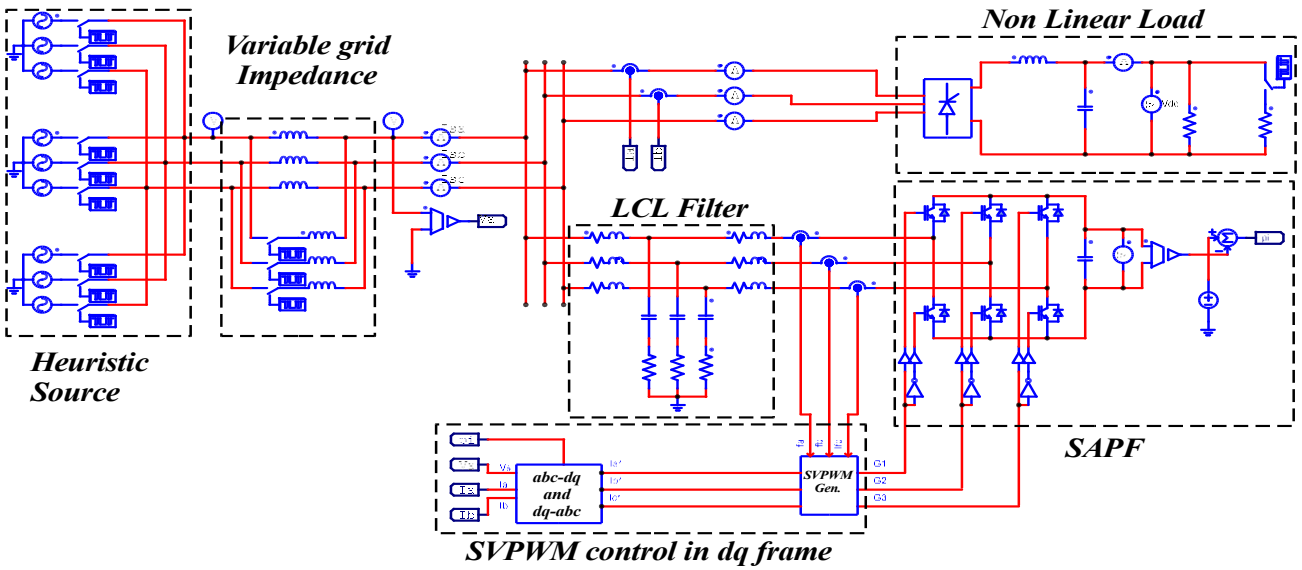

Figure 6. Simulation Test Bench

The simulation, as shown in *fig.7*, is carried out with

- perturbations applied at every half of the second in load, which vary from 2.23Ω (45.2 Kw) to 4.46Ω (135 Kw).
- Variation in grid impedance from 0.3 mH to 1.0 mH, takes place every second.
- Source voltage is varied after every two seconds in the range of 415 ±20% (332V - 415V - 498V)
- Frequency of the source is varied from 48 Hz to 50 Hz to 52 Hz. This variation is also applied along with the variation in the voltage.

These variations have been mapped with time in the *table 5*, as well.

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

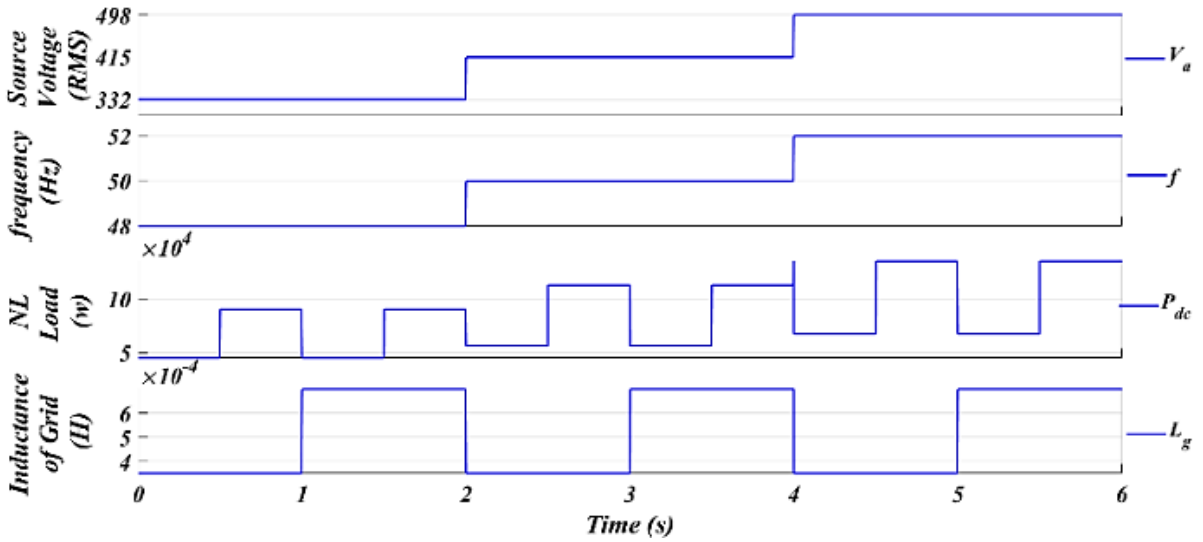

Figure 7. Perturbations in Grid voltage, Frequency, Load, and Impedance of the Grid

Here, the considered system is of a *3-ϕ 3-wire* type, where, as a measure of cost cutting, the samples of *2-ϕ* currents from PCC, *2-ϕ* currents at the output of the VSC, and the voltage of the DC-bus are fetched to the controller. The remaining third phase current can be derived from the available currents. Here, the purpose is to comply with the IEEE-519 standard [0] by reducing the THD below 5% and setting the power factor close to 1 so as to reduce the reactive power.

6. RESULTS AND ANALYSIS

The effectiveness of the proposed control strategy has been validated through comparison with the same system operating under a sinusoidal pulse-width modulated (SPWM) SAPF. Here, the non-linear load has been made more stringent by deliberately debilitating its filter's performance in the case of SVPWM control, with parameters set to L_{dc}=0.5 mH and C_{dc}=500 µF. This adjustment was intended to drive a higher level of harmonic distortion (% THD) towards the PCC, as is evident from *table 5*.

Fig.8 presents the absolute spectrum of 6s of simulation, and it incorporates variation in current at PCC and before PCC, voltage at PCC, DC-bus voltage profile o SAPF, and a voltage emanated by the source. We barely find any larger transient peaks in any of the plots, at the wake of change in the perturbing parameters.

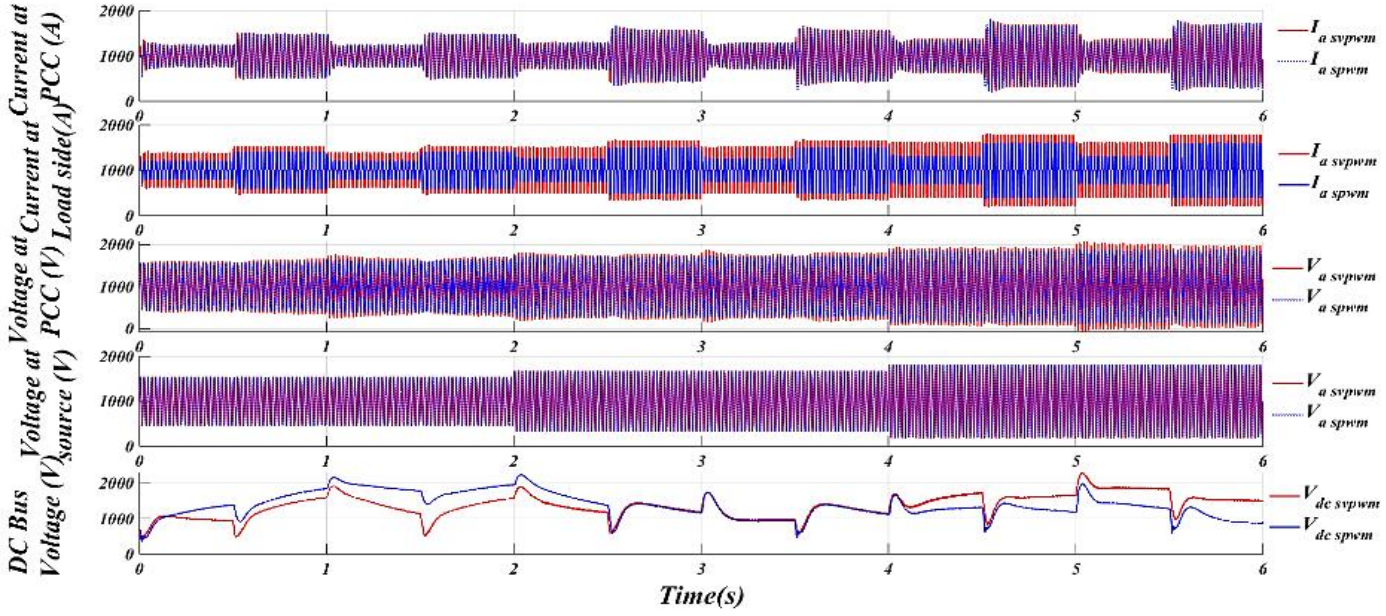

Figure 8. Instantaneous values of current and voltages at PCC, harmonically molested current between PCC and non-linear load, DC-bus voltage of SAPF, and perturbing Grid Voltage having frequency variation

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

The Fast Fourier Transform (FFT) of the complete spectral results shown in *fig. 8* is presented in *fig. 9* to confirm the presence of three distinct frequency components. This observation is further substantiated by the appearance of three prominent peaks in each spectral window. The phase current (I_a), measured between the PCC and the load, clearly exhibits higher harmonic components in the case of SVPWM control, occurring at integer multiples of the corresponding fundamental frequencies.

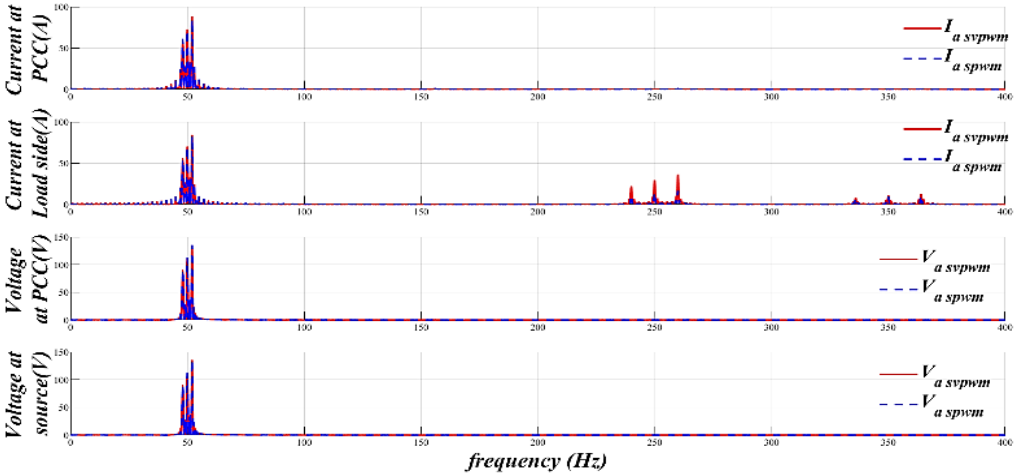

Figure 9. FFT analysis of parameters presented in *figure 8*

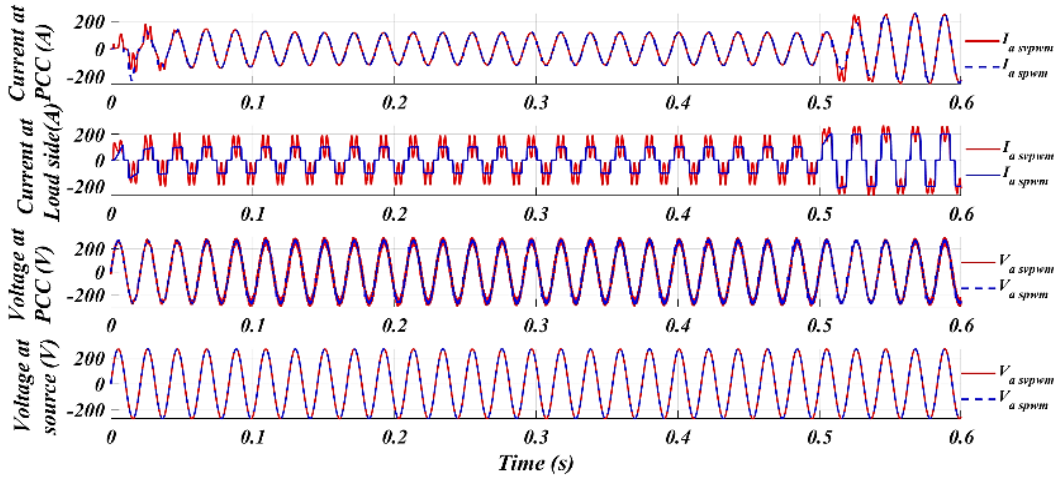

Figure 10. Parameters of Fig.8 sampled between 0 to 0.6s, showing a startup instance.

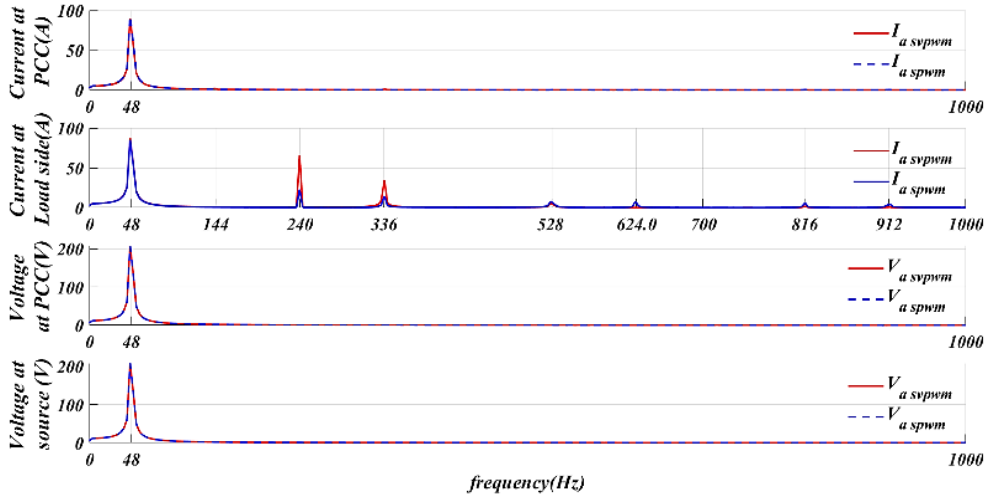

Figure 11. FFT analysis of parameters presented in *fig. 10* (for the spectrum of 0 to 0.5 s)

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

Fig.10 shows the fast and efficient response of the ePLL, which is extracting a perfect voltage reference from the distorted one (due to a weak grid, the harmonics in the current are causing further molestation of the voltage) in less than two cycles from the initial startup. I_a, measured between the PCC and the load, appears discontinuous in the case of SVPWM, with the Total Harmonic Distortion (THD) varying between 34.1% and 76.7%. In contrast, under SPWM, the current exhibits a quasi-square waveform with THD ranging from 27.7% to 29.6%. These observations are corroborated by the data presented in *table 5*. The same is evident from the FFT spectrum of the same presented in *fig.11*, revealing higher 5th and 7th order harmonics in the case of SVPWM control, while maintaining a matching fundamental current at the PCC.

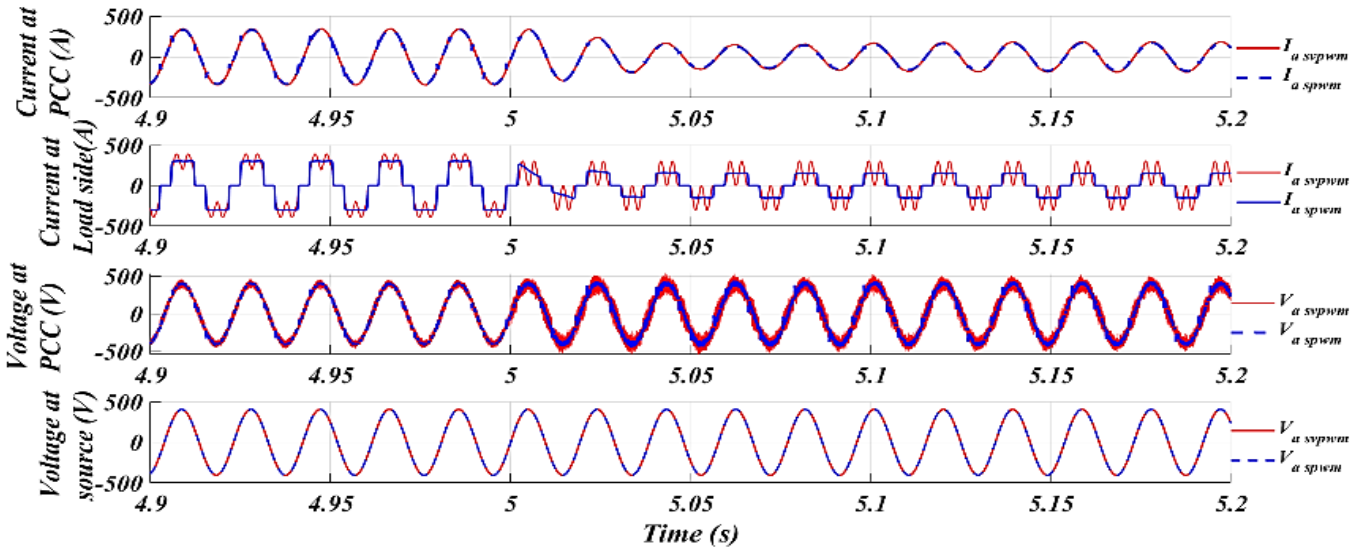

Figure 12. Transitions at the wake of a change in voltage, frequency, load, and grid reactance

Figure 12 shows a transitional event where the voltage, frequency, load, and grid reactance are altering at the instance of 2s. We could see a transient and distortion-free transition in I_a at PCC without any considerable delay, in both the cases.

Table 5. Comparative Result Analysis

Time (s)	*f (Hz)*	*V_a (rms)*	*L_g (mH)*	*P_{dc} (Kw)*	*%THD in I_{aSVPWM}*	*%THD in I_{aSPWM}*	*%THD in I_{LSVPWM}*	*%THD in I_{LSPWM}*	*%THD in V_{aSVPWM}*	*%THD in V_{aSPWM}*	*P.F. with SVPWM*	*P.F. with SPWM*
0 to 0.5	48	191	3.5	45.2	2.2	3.5	66.4	29.6	10.4	5.4	0.995	0.998
0.5 to 1.0	48	191	7	90.4	2.1	3.1	34.1	29.2	18.1	7.8	0.999	0.999
1.0 to 1.5	48	191	3.5	45.2	2.2	3.0	67.1	29.3	20.0	10.3	0.998	0.998
1.5 to 2.0	48	191	7	90.4	1.8	2.5	34.2	28.8	27.3	12.2	0.999	0.997
2.0 to 2.5	50	240	3.5	56.4	2.1	3.8	75.7	29.6	10.1	4.7	0.999	0.997
2.5 to 3.0	50	240	7	112.7	2.2	4.4	35.0	28.8	10.8	5.4	0.997	0.995
3.0 to 3.5	50	240	3.5	56.4	1.8	3.4	76.7	29.2	12.6	5.7	0.998	0.995
3.5 to 4.0	50	240	7	112.7	1.6	3.4	35.2	28.4	16.3	8.2	0.994	0.990
4.0 to 4.5	52	288	3.5	67.6	2.5	4.1	75.2	29.5	13.2	4.1	0.998	0.997
4.5 to 5.0	52	288	7	135	2.3	5.3	35.4	28.5	12.6	5.2	0.995	0.994
5.0 to 5.5	52	288	3.5	67.6	2.3	3.3	75.2	29.1	21.9	6.3	0.998	0.996
5.5 to 6.0	52	288	7	135	1.8	5.9	35.2	27.7	18.1	7.2	0.992	0.990

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942|e-ISSN: 2347-470X

The comparative results presented in *table 5* reveal that SVPWM consistently achieves lower current distortion in I_a compared to SPWM, with %THD values remaining between 1.6–2.5% versus 2.5–5.9% (gross violation of IEEE 529), in the presence of significantly higher distortion in I_L under SVPWM, often exceeding 65–75% compared to 30% with SPWM. Higher distortion in I_a with SVPWM is the cause of greater distortion in V_a (10–28% THD) compared to only 5–13% in SPWM. Moreover, the power factor with SVPWM is marginally better compared to that of SPWM. Settling time in all the cases of perturbing instances of changeover is less than 4ms, as could be witnessed from *fig. 8*, *fig. 10*, and *fig.12*. Overall, SVPWM is more effective at minimizing source current THD and enhancing power quality at the grid interface.

7. REAL TIME IMPLEMENT ABILITY

Real-time implement ability of the Shunt Active Power Filter (SAPF) depends on how efficiently its control algorithms and hardware can respond to dynamic grid conditions. With the PI–SVPWM strategy, the system achieves fast current tracking and effective harmonic compensation, ensuring that corrective signals are generated within each switching cycle. The use of an LCL filter with proper damping further stabilizes the response, making the SAPF robust against grid variations. Considering the computational burden of controller implementation—which requires *abc-to-dq* transformation and fixed-frequency SVPWM control—a low-latency floating-point digital signal processor (DSP), such as the Texas Instruments TMS320F28379D, is essential for real-time operation. Moreover, the solution must remain cost-effective. In addition, the use of precision Hall-effect current sensors (*e.g.*, Allegro ACS713) ensures reliable power quality improvement without introducing computational delays.

8. CONCLUSION

This work demonstrated the design and validation of a robust yet simple, shunt active power filter, being controlled through Space Vector PWM (SVPWM), operating in the microgrid framework. The optimal LCL filter achieves exceptional harmonic attenuation (>50 dB at 20 kHz), surpassing LC filter performance, with effective passive damping and a compact footprint. This has been validated through a thorough comparison of SVPWM with Sinusoidal PWM (SVPWM) control for the same system of grid condition, but with a more stringent nonlinear load proliferating more harmonics for the SVPWM control.

Cascaded PI controllers in the synchronous reference frame provide precise DC voltage regulation and accurate harmonic tracking up to 1250 Hz, while offering flexibility for reactive power compensation through (I_q^*) adjustment. As evidenced in *table 5*, the proposed SAPF achieves a substantial reduction in source current THD, lowering it from 34.1–76.7% to 1.6–2.5%, even under distorted grid voltages where (V_a) THD ranges between 10–28%. The system maintains a near-unity power factor of 0.99, demonstrating compliance with IEEE-519 standards across diverse load and grid conditions. These results confirm that the designed SAPF and its cascaded PI–SVPWM controller not only ensure grid-side harmonic suppression but also exhibit robustness and reliability, thereby validating the efficacy of the proposed control strategy for real-time power quality enhancement.

Author Contributions: Conceptualization, Mehul Dansinh Solanki; methodology, Mehul Dansinh Solanki; validation, Mehul Dansinh Solanki, and Ashok Kumar Parmar and Jaydeepsinh Sarvaiya; formal analysis, Mehul Dansinh Solanki; writing—review and editing, Mehul Dansinh Solanki, Mayur Gojiya; visualization, Mehul Dansinh Solanki; supervision, S. K. Joshi; All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

REFERENCES

[1] M. Ali, M. Yaqoob, L. Cao, and K. H. Loo, "Enhancement of DC-bus voltage regulation in cascaded converter system by a new sensorless load current feedforward control scheme," IET Power Electronics, vol. 14, no. 8, pp. 1457–1467, Jun. 2021. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/full/10.1049/pel2.12123

[2] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," IEEE Trans. Power Electron., vol. 24, no. 3, pp. 654–664, Mar. 2009. [Online]. Available: https://ieeexplore.ieee.org/document/4801680

[3] H. M. Kojabadi, B. Yu, I. A. Gadoura, L. Chang, and M. Ghribi, "A novel DSP-based current-controlled PWM strategy for single phase grid connected inverters," IEEE Trans. Power Electron., vol. 21, no. 4, pp. 985–993, Jul. 2006. [Online]. Available: https://ieeexplore.ieee.org/document/7869729

[4] J. N. da Silva, A. J. Sguarezi Filho, D. A. Fernandes, A. P. Tahim, E. R. da Silva, and F. F. Costa, "A discrete repetitive current controller for single-phase grid-connected inverters," in Proc. Brazilian Power Electron. Conf. (COBEP), Nov. 2017, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/document/8257339

[5] S. K. Pati, P. K. Sahu, and S. Jena, "Power quality enhancement of shunt active power filters by sliding mode control technique," in Advances in Intelligent Computing and Communication, ICAC 2024, Lecture Notes in Networks and Systems, vol. 1325, M. N. Mohanty and S. Das, Eds. Singapore: Springer, 2025. [Online]. Available: https://doi.org/10.1007/978-981-96-4071-3_30

[6] V. Narasimhulu, D. V. Ashok Kumar, and C. Sai Babu, "Fuzzy logic control of SLMMC-based SAPF under nonlinear loads," Int. J. Fuzzy Syst., vol. 22, pp. 428–437, 2020. [Online]. Available: https://doi.org/10.1007/s40815-019-00622-0

[7] M. Caoyuan, L. Gang, L. Jianhua, W. Chonglin, W. Zhi, and Z. Wanyun, "The space vector control of the SAPF in the condition of non-ideal source," in Proc. Int. Conf. Mechanic Autom. Control Eng., Jun. 2010, pp. 4006–4009. [Online]. Available: https://doi.org/10.1109/MACE.2010.5535914

[8] L. F. Monteiro, J. L. Afonso, J. G. Pinto, E. H. Watanabe, M. Aredes, and H. Akagi, "Compensation algorithms based on the pq and CPC theories for switching compensators in micro-grids," in Proc. Brazilian Power Electron. Conf., Sep. 2009, pp. 32–40. [Online]. Available: https://ieeexplore.ieee.org/document/5347593

[9] C. C. Gomes, A. F. Cupertino, and H. A. Pereira, "Damping techniques for grid-connected voltage source converters based on LCL filter: An overview," Renew. Sustain. Energy Rev., vol. 81, pp. 116–135, Jan. 2018. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1364032117311206

[10] Y. Wang, J. Z. Liu, and X. T. Xu, "Study of a new grid-connected LCL filter for shunt active power filter," in Proc. IEEE Conf. Expo Transp. Electrification Asia-Pacific (ITEC Asia-Pacific), Aug. 2014, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/document/6940955

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 4 | Pages 932-942 | e-ISSN: 2347-470X

[11] D. Khan, P. Hu, S. Habib, M. Waseem, Z. Lin, and E. M. Ahmed, "A resonant damping control and analysis for LCL-type grid-connected inverter," Energy Reports, vol. 8, pp. 911–928, Nov. 2022. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2352484721014207

[12] M. D. Solanki and S. K. Joshi, "Robust and novel carrier based unipolar space vector pulse width modulation control of single-phase electric spring, using a lead-lag compensator," Comput. Electr. Eng., 2024. [Online]. Available: https://doi.org/10.1016/j.compeleceng.2024.109692

[13] M. Karimi-Ghartema, Enhanced Phase-Locked Loop Structures for Power and Energy Applications. Hoboken, NJ, USA: John Wiley & Sons, Mar. 2014.

[14] P. C. Krause, O. Wasynczuk, S. D. Sudhoff, and S. Pekarek, Analysis of Electric Machinery and Drive Systems. New York, NY, USA: IEEE Press, Feb. 2002.

[15] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1281–1291, 2005. doi: 10.1109/TIA.2005.853373

[16] Analog Devices, "Chapter 8 analog filters," in Basic Linear Design Handbook. Norwood, MA, USA: Analog Devices, Inc., 2012. [Online]. Available: https://www.analog.com/media/en/training-seminars/design-handbooks/basic-linear-design/chapter8.pdf

[17] IEEE Standard for Harmonic Control in Electric Power Systems, IEEE Std 519-2022 (Revision of IEEE Std 519-2014), pp. 1–31, Aug. 2022. doi: 10.1109/IEEESTD.2022.9848440