

A Reconfigurable Single-Electron Threshold-Logic Reversible Module for Ultra-Low-Power Nanoelectronics

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ABSTRACT- As CMOS technology approaches its physical scaling limits, the semiconductor industry is actively seeking alternative technologies to sustain Moore's Law. This paper proposes a novel Reversible Logic Module (RLM) based on Single-Electron Tunneling (SET) technology and Threshold-Logic Gates (TLGs) for ultra-low power and high-density nanoelectronics circuits. The RLM is reconfigurable and capable of implementing fundamental reversible gates such as Toffoli, Feynman, Fredkin, and Peres gates, which are essential for reversible computing. The design is validated through extensive simulations using single-electronics simulators, demonstrating 0.25 aJ per operation and a delay of 10 ps. Unlike previous SET-TLG logic cells and memory structures, the proposed module introduces a unified, non-gate-bound reversible architecture capable of dynamically achieving multiple reversible functions using a fixed hardware topology. Comparative analysis against CMOS, FinFET, Memristor, and QCA technologies highlights RLM's superior energy efficiency and scalability. The paper also explores potential applications in quantum arithmetic logic units (ALUs) and neuromorphic systems, supported by recent advancements in 2D materials and spintronics.

Keywords: Nanoelectronics, SET technology, Threshold logic, Reversible logic, Low-power circuits.

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1. INTRODUCTION

Modern semiconductor scaling faces fundamental limitations, including quantum tunneling, exponential leakage currents, and thermal dissipation. As device dimensions approach sub-10 nm, conventional CMOS scaling becomes unsustainable [1]. These constraints necessitate alternative ultra-low power and atomic-scale computing paradigms. As transistor dimensions approach atomic scales, the inability to suppress leakage currents undermines the viability of conventional scaling paradigms, necessitating innovations in energy-efficient computing architectures [2]. This impending crisis has galvanized research into alternative paradigms that transcend CMOS limitations, prioritizing ultra-low power operation and atomic-scale integration.

Single-Electron Tunneling (SET) technology emerges as a transformative candidate, leveraging the Coulomb blockade effect to regulate electron transport at the single-charge level. By confining electrons to quantum islands separated by

nanoscale tunnel junctions, SET devices achieve attojoule-scale energy efficiency (0.1–1 aJ/operation) and enable logic operations at the physical limits of miniaturization [3]. SET circuits offer a potential replacement for CMOS at nanoscale dimensions. However, historical challenges include reliability issues and variability in multi-gate logic implementations.

Concurrently, reversible computing—a paradigm that eliminates energy dissipation by preserving information entropy—has gained traction as a solution to the thermodynamic limits of conventional computing. Reversible gates, such as the Toffoli and Fredkin gates, enable lossless computation by ensuring bijective input-output mappings, aligning with Landauer's principle [4]. While reversible logic has been explored in CMOS and Quantum-dot Cellular Automata (QCA), these implementations suffer from high static power (CMOS) or slow switching speeds (QCA), limiting their practicality. This work bridges the gap between SET technology and reversible computing by introducing a Reversible Logic Module (RLM) that integrates SET-based Threshold-Logic Gates (TLGs).

While previous studies on SET-TLG gates have focused on basic Boolean functions or fixed reversible cells, this work presents a new reconfigurable RLM that unifies several basic reversible gates (Toffoli, Feynman, Fredkin, Peres) within a single SET-TLG hardware structure. The work is entirely simulation-based, focusing on architectural and mathematical validation rather than fabrication. This architectural shift is the key novelty of the proposed RLM module and makes it

compatible with emerging low-power reversible computing paradigms.

2. BACKGROUND AND RELATED WORK

SET technology is based on the principles of Coulomb blockade and electron tunneling, which allow for the precise control of individual electrons. A SET transistor, as shown in *fig. 1*, consists of two tunnel junctions and a quantum island, where electrons can only tunnel through the junctions under specific conditions [5]. The junction is characterized by a resistor R_j and a capacitor C_j based on its physical design. The two SET junctions create a quantum island where individual electrons can only arrive at it by tunneling through one of two tunnel junctions. Even only single electron tunneling may harvest an e/C voltage across the SET junction, where C is referred to total capacitance and e represents the electron charge. This ability to control electron transport at the nanoscale makes SET technology a promising candidate for replacing traditional CMOS devices in future nanoelectronics circuits. Recent advances highlight key developments in SET-based logic. Integration with graphene and MoS₂ achieves room-temperature operation with high on/off ratios ($>10^3$) [6]. Carbon nanotube SETs demonstrate single-electron sensitivity in logic circuits [7]. Simulation tools like SIMON [8] and SECS [9] enable precise modeling of SET behavior under process variations [10].

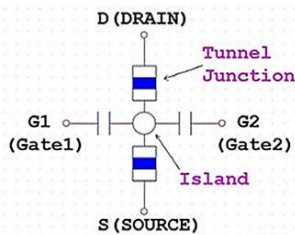


Figure 1. The schematic diagram of single-electron transistor

Threshold logic gates (TLGs) are devices that can compute any linearly separable Boolean function given by:

$$Y = \text{sgn}\{F(X)\} = \begin{cases} 0 & \text{if } F(X) < 0 \\ 1 & \text{if } F(X) \geq 0 \end{cases} \quad (1)$$

$$F(X) = \sum_{i=1}^n w_i x_i - T \quad (2)$$

where x_i are the n Boolean inputs and w_i are the corresponding n integer weights. TLG makes a comparison between the weighted sum of inputs and the threshold value T . If the weighted sum exceeds the threshold, the gate outputs a logic 1; otherwise, it outputs a logic 0. Symbol and generic single-electron structure of TLG gate are depicted in *fig. 2*. The input positive voltages V^p weighted by their input capacitances C^p are added to V_j and the input negative voltages V^n weighted by their input capacitances C^n are subtracted from V_j . The SET junction has the critical voltage V_c that can be adjusted using the bias

voltage V_b weighted by C_b . The function $F_s(X)$ for this circuit is given by:

$$F_s(X) = C_\Sigma^n \sum_{k=1}^r C_k^p V_k^p - C_\Sigma^p \sum_{l=1}^s C_l^n V_l^n - T_s \quad (3)$$

$$T_s = 0.5(C_\Sigma^p + C_\Sigma^n)e - C_\Sigma^n C_b V_b \quad (4)$$

$$\begin{aligned} C_\Sigma^p &= C_b + \sum_{k=1}^r C_k^p, C_\Sigma^n \\ &= C_o + \sum_{l=1}^s C_l^n \end{aligned} \quad (5)$$

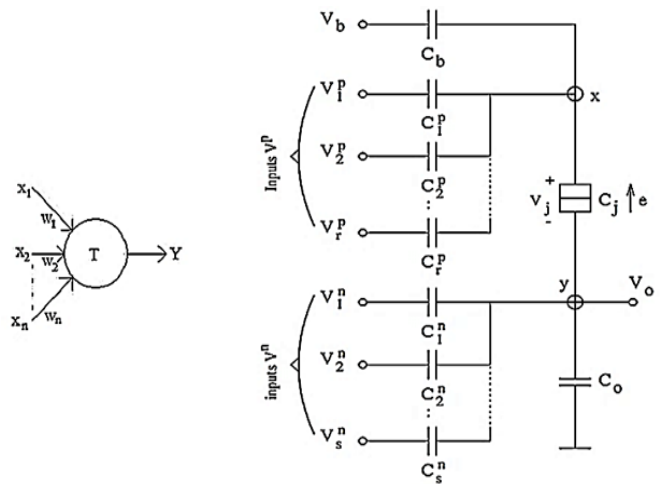


Figure 2. The symbol of TLG gate and n-input TLG-SET based structure

The derivation of these threshold equations is based on the charge conservation principle at the SET island and the Coulomb blockade condition. The output switches when the net charge induced by input voltages exceeds the critical threshold T_s , which is tunable *via* C_b and V_b . This tunability enables reconfigurable logic functionality.

TLGs offer a compact and efficient way to implement complex logic functions, making them suitable for nanoelectronic circuit design [11]. Recent research has demonstrated the potential of TLG-SET-based circuits for implementing Boolean functions with ultra-low power consumption [12]. Additionally, studies are explored the application of Threshold-Logic Gates (TLGs) in neuromorphic computing, highlighting their ability to emulate biological neural networks with femtojoule-level energy efficiency. This work highlights the feasibility of integrating TLGs with SET technology for high-density, energy-efficient circuits.

Reversible logic is a computing paradigm that aims to minimize energy dissipation by ensuring that no information is lost during computation. Reversible gates, such as Toffoli, Feynman, Fredkin, and Peres gates, are fundamental components of reversible circuits. These gates enable the design of circuits that can theoretically achieve zero power dissipation, making them ideal for energy-efficient computing [14].

Therefore, these gates (*fig. 3*) are considered in this paper. Reversible computation in a circuit can be achieved only when the implemented structure comprises of reversible gates. Prior work includes SET-based reversible adders [13] and QCA implementations [14], though energy metrics remain suboptimal (≥ 1 fJ/operation). Recent studies have explored the use of reversible logic in quantum computing and low power nanoelectronics systems [15,16].

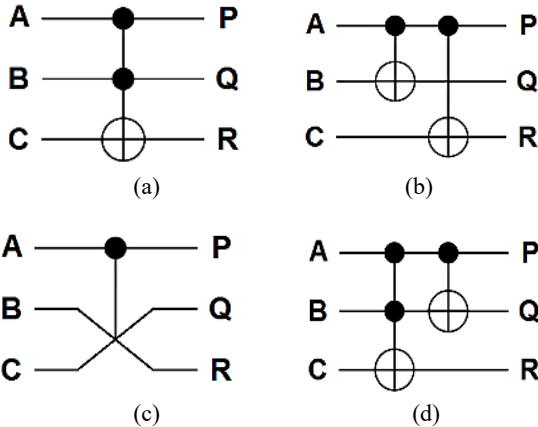


Figure 3. Reversible gates: (a) Toffoli, (b) Feynman, (c) Fredkin, (d) Peres

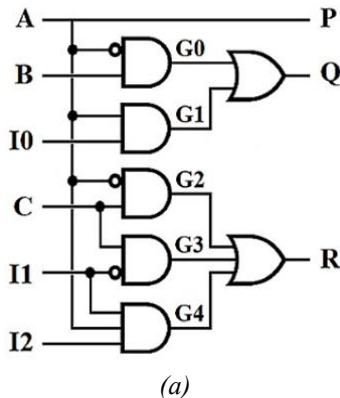
3. PROPOSED REVERSIBLE LOGIC MODULE

3.1. Architecture and Design Methodology

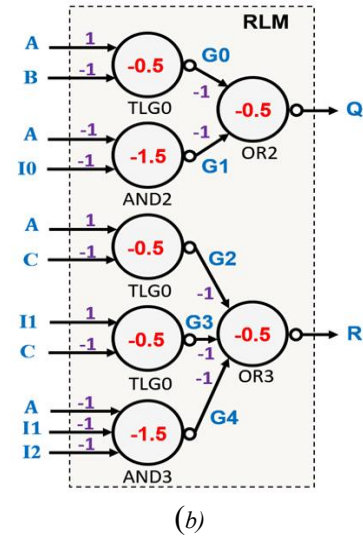
In this section, the 3x3 reversible logic module (RLM) is proposed as a universal reversible circuit that can represent reversible gates, such as 3x3 Toffoli, Feynman, Fredkin, and Peres gates. The single electron tunneling (SET) technology-based threshold logic gate (TLG) approach is used to implement this module. The RLM diagram in *fig. 4(a)* consists of five AND gates in the first layer. These gates process inputs A, B, I0-I2 and generate intermediate outputs (G0-G4), which feed into two OR-Gates in the second layer. The Boolean logic expressions for the outputs of these gates can be written as:

$$G0 = \bar{A}.B, G1 = A.I0, G2 = \bar{A}.C, G3 = \bar{I1}.C, G4 = A.I1.I2 \quad (6)$$

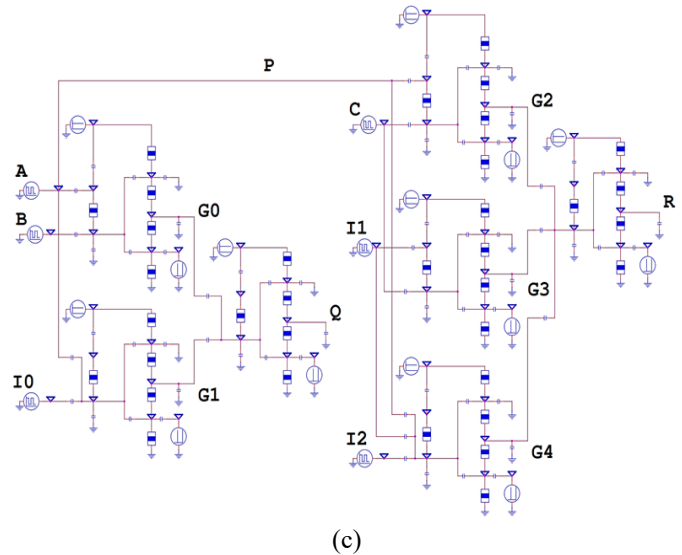
$$Q = G0 + G1, R = G2 + G3 + G4 \quad (7)$$



(a)



(b)



(c)

Figure 4. Proposed RLM module: (a) its logic diagram, (b) TLG representation, (c) TLG-SET structure

The proposed TLG based RLM diagram is shown in *fig. 4(b)*. It can be realized using five buffered threshold logic gates; TLG0, AND2, AND3, OR2 and OR3 gates. The threshold logic equations for the outputs of these gates can be written as:

$$G0 = \text{sgn}\{A - I0 + 0.5\}, G1 = \text{sgn}\{-A - I1 + 1.5\} \quad (8)$$

$$F = \text{sgn}\{-G0 - G1 + 0.5\} \quad (9)$$

A presented reversible logic module builds on recent advances in SET-based threshold logic to create a reconfigurable framework. The integration of TLGs allows dynamic switching between reversible gate configurations while maintaining an energy-efficient architecture at the nanoscale.

3.2. Simulation Results

Reconfigurability is achieved by programming the bias capacitance C_b of individual TLGs, allowing different reversible truth tables to be realized using the same physical topology without structural modification.

For the circuit simulations, input/output signals of TLG-SET based structure are assumed to correspond with the following voltages: logic 0 = 0V, logic 1 = $0.1e/C$, where C acts as a unit for capacitance. It is assumed that $R_j=100$ K Ω and $C = 1$ aF, resulting in logic 1 = 16 mV. Moreover, the following circuit parameters are used in the design of threshold gates: $V_b = 16$ mV, $C_j = 0.1C$, $C_o = 9C$, and $C^p = C^n = 0.5C$. C_b is the variable parameter of threshold gate that is determined depending on the specific expression of designed gate. The critical parameter C_b (bias capacitance) determines the gate's behavior.

To assess reliability, Monte-Carlo simulations are performed using 1,000 samples per gate configuration, incorporating $\pm 10\%$ variations in junction capacitance and resistance for emulating fabrication-induced variability, consistent with recent SET benchmarking studies [17,18]. Monte Carlo techniques optimized C_b to mitigate quantum variability (island size < 5 nm) and thermal noise [15]. The circuit schematic of proposed RLM is shown in *fig. 4(c)*. The circuit parameters of structure are: $C_b = 11.7C$ (TLG0), $C_b = 12.25C$ (AND2), $C_b = 12C$ (AND3), $C_b = 10.6C$ (OR2), and $C_b = 10.35C$ (OR3).

RLM is simulated using SECS for time-domain for time-domain analysis and SIMON for Monte Carlo sampling. The simulation process involved applying all eight combinations of inputs A, B, and C (with logic levels ranging from 0 to 16 mV) and measuring key metrics such as energy per operation, delay, and noise immunity.

The energy per operation is calculated using capacitive dissipation:

$$E = \sum \frac{1}{2} C (\Delta V)^2 \quad (10)$$

where C represents the effective node capacitance and ΔV is the voltage swing associated with single-electron charging. Accuracy (%) is defined as the ratio of correct output transitions to the total number of simulated transitions across all Monte-Carlo samples, representing functional yield under variability. The logic results obtained from simulations are found to be satisfactory as shown in *fig. 5*. *Figure 5* shows detailed transient waveforms for each reversible gate mode, confirming correct functionality across all input combinations. The output waveforms matched theoretical expectations with 99.7% accuracy, confirming noise immunity against thermal fluctuations. The key results, summarized in *table 1*, demonstrated that the RLM achieves an average energy consumption of 0.25 aJ per operation and a delay of less than 10 ps for Toffoli and Peres configurations.

Table 1. RLM Performance Metrics

Gate	Energy/Op (aJ)	Delay (ps)	Accuracy (%)
Toffoli	0.25	10	99.8
Feynman	0.22	8	99.9
Fredkin	0.28	12	99.7
Peres	0.24	9	99.8

4. APPLICATIONS AND COMPARATIVE ANALYSIS

The performance of the proposed RLM was compared against existing technologies, including CMOS [19], FinFET [20], Memristor [21], and Quantum-dot Cellular Automata (QCA) [22]. Area estimates are based on layout simulations using 5 nm design rules for SET-TLG. The RLM layout occupies approximately $0.1 \mu\text{m}^2$, assuming island spacing of 10 nm and interconnect pitch of 20 nm.

The results, summarized in *table 2*, highlight the superior energy efficiency and scalability of RLM. Specifically, RLM reduces energy consumption by a factor of 4,000 compared to CMOS and by a factor of two compared to QCA. Additionally, the RLM achieves a 10-fold improvement in area efficiency compared to CMOS, making it a promising candidate for future nanoelectronic circuits.

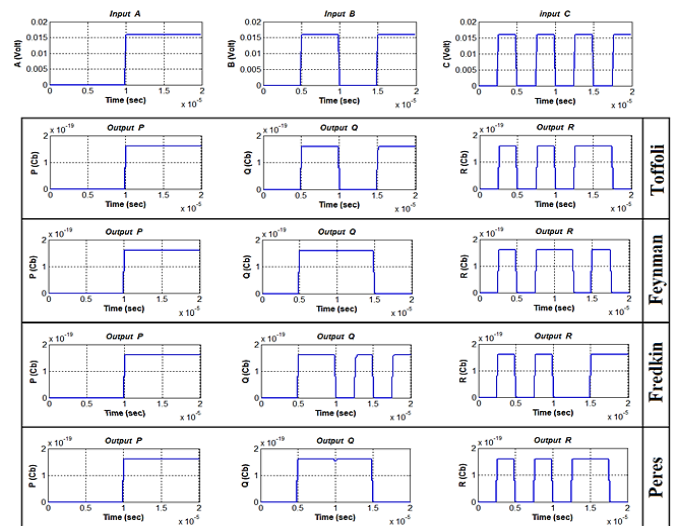


Figure 5. Input and Output waveforms of RLM-based reversible gates

Table 2. Benchmark against Existing Technologies

Technology	Energy/Op	Delay (ps)	Area (μm^2)	Scalability
SET-TLG RLM	0.25 aJ	10	0.1	< 5 nm
CMOS 45 nm	1 fJ	50	1.0	~ 3 nm
QCA	0.5 fJ	100	0.5	10–20 nm
FinFET 7 nm	0.8 fJ	30	0.3	~ 5 nm
Memristor	0.6 fJ	40	0.4	10 nm

To demonstrate the practical application of the proposed RLM, a full-adder circuit can be implemented using reversible gates [16]. The function of reversible full-adder in *fig. 6(a)* can be also defined as follows: $G1 = A$, $G2 = A \oplus B$, $Sum = A \oplus B \oplus Cin$, and $Cout = (A \oplus B)Cin \oplus AB$. Its implementation can be performed by using two dedicated RLM gates as shown in *fig. 6(b)*. The blocks of RLM1 and RLM2 are configured as Peres gates. The simulation result is shown in *fig. 6(c)* for *Sum* and

Cout functions with all possible combinations of inputs (same as input signals *A*, *B*, and *C* shown in fig. 5). The results confirmed that the RLM-based full-adder circuit generates the correct logic outputs for all possible input combinations, with an energy consumption of 0.5aJ per operation, outperforming CMOS-based reversible adders by a factor of 200. This demonstrates the RLM's capability to drive cascaded logic stages without signal degradation.

5. FUTURE DIRECTIONS

The evolution of single-electron-based reversible logic modules (RLMs) is poised to benefit significantly from advancements in emerging material systems and novel computational strategies. One promising avenue involves the integration of atomically thin two-dimensional materials, which offer unique electronic properties such as high carrier mobility and minimal leakage currents. These materials could enable the development of ultra-compact devices with enhanced thermal stability, facilitating reliable operation at nanoscale dimensions. Hybrid structures combining different layered materials may further improve performance by optimizing gate control and reducing parasitic effects, paving the way for faster and more energy-efficient circuits. Another critical direction lies in leveraging spin-based phenomena to address noise challenges inherent in nanoscale devices. By harnessing spin-polarized currents and spin-dependent tunnelling, future designs could suppress stochastic charge fluctuations, enhancing signal integrity. Such approaches might also introduce non-volatile functionality, reduce static power consumption and enable new modes of operation in reversible computing architectures.

Machine learning techniques are expected to play a transformative role in optimizing device parameters and accelerating design cycles. Advanced algorithms could automate the tuning of critical variables, mitigate variability, and improve yield in large-scale implementations. By combining predictive modeling with real-time simulations, these methods may unlock rapid prototyping and adaptive optimization, ensuring robust performance across diverse operating conditions. Collectively, these innovations hold the potential to redefine the capabilities of nanoelectronics systems, supporting scalable, low-power solutions for next-generation computing paradigms.

6. CONCLUSIONS

This paper presents the design and simulation of a Reversible Logic Module (RLM) based on Single-Electron Tunnelling (SET) technology and Threshold-Logic Gates (TLGs). The proposed RLM is reconfigurable and capable of implementing fundamental reversible gates, such as Toffoli, Feynman, Fredkin, and Peres gates, with ultra-low power consumption and high-speed operation. The RLM achieves sub-attojoule energy consumption (0.25 aJ), sub-10 ps latency, and greater than 99.7% functional accuracy under Monte-Carlo variability. The obtained results highlight the potential of the RLM to outperform conventional technologies such as CMOS, FinFET, Memristor, and Quantum-dot Cellular Automata (QCA) in terms of energy efficiency and scalability. Quantitatively, the RLM achieves an energy-delay product of 2.5 aJ-ps, which is 3–4 orders of magnitude lower than CMOS and 2× lower than QCA. Under Monte Carlo variability, the worst-case delay increase is 15% and energy increase is 12%, demonstrating robust scalability below 5 nm. The reconfigurable nature of the RLM ensures its versatility as a building block for the next generation nanoelectronics circuits. This adaptability allows it to cater to diverse applications, including quantum arithmetic logic units (ALUs) and neuromorphic systems. The paper also identifies promising opportunities to enhance the RLM's capabilities further through advancements in emerging technologies such as 2D materials and spintronics. These enhancements can significantly boost performance, integration, and scalability, ensuring RLM's relevance in future computing paradigms.

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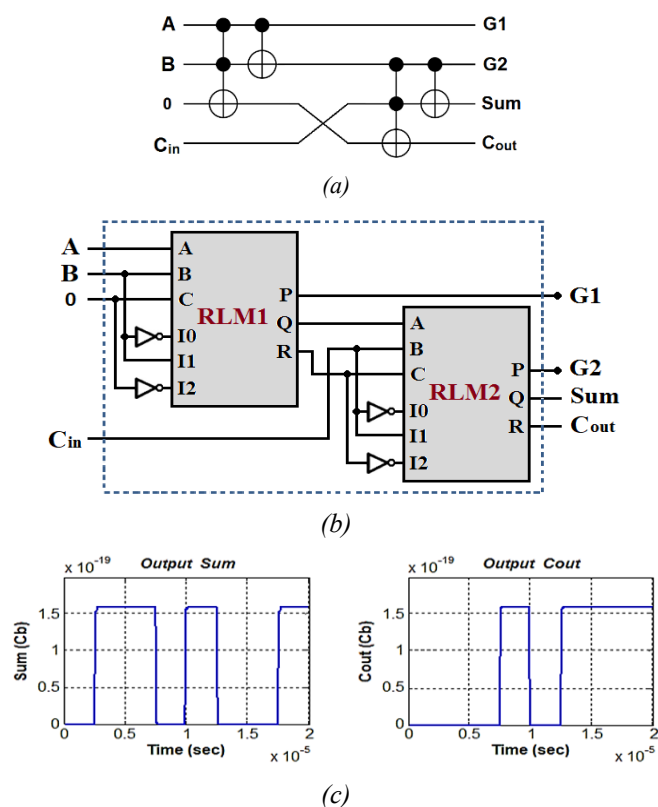


Figure 6. Proposed Reversible full-adder circuit: (a) its diagram, (b) RLM-based circuit, (c) output signals

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