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Real-Time Implementation of dSPACE DS1104 to a Full-Bridge DC-DC Converter with EMI Mitigation

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ABSTRACT- A conventional isolated full-bridge (FB) DC–DC converter for electric vehicle (EV) battery charger is implemented and experimentally validated using a real-time digital control platform based on the dSPACE DS1104 controller presented in this paper. The proposed charger is designed to deliver a regulated output of 56 V at 15 A for charging a 48 V lithium-ion battery pack. This work focuses on practical power-stage design with appropriate semiconductor device selection, high-frequency transformer design, output filter design considering switching stress mitigation. To address electromagnetic interference (EMI) in full-bridge converters due to high dv/dt and di/dt switching transitions, a passive mitigation approach with an input capacitor and RC snubber network is presented. This method reduces voltage overshoot and switching stress without increasing control or circuit complexity. A PI-based voltage control strategy is implemented on the dSPACE DS1104 platform for real-time PWM generation, closed-loop regulation and direct observation of converter dynamics during operation. The proposed system is validated through simulation and experimental testing results demonstrating stable output regulation, reduced switching stress and improved EMI behaviour. The results highlight the suitability of dSPACE-based real-time control for rapid prototyping and experimental investigation of power stages for isolated EV charger. The study provides practical implementation insights and a systematic design reference for researchers and engineers working on real-time EV battery charger development.

Keywords: Full-Bridge DC–DC Converter, dSPACEDS1104, electromagnetic interference, electric vehicle (EV) charger, real-time digital control.

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1. INTRODUCTION

The worldwide transition toward environmentally friendly transportation has significantly accelerated the adoption of electric vehicles (EVs). A vital component of an EV is the battery charger, which plays a critical role in determining overall efficiency, safety, and reliability. EV battery chargers are expected to be efficient, compact, cost-effective, and capable of precise voltage and current regulation. From a safety point of view, the charger should be able to provide galvanic isolation and comply with electromagnetic compatibility (EMC) requirements to ensure reliable operation and user protection [1]– [3].

In the Indian context, the swift expansion of electric two-wheelers manufactured by companies such as Ather Energy, Ola Electric, TVS Motor Company (iQube), Bajaj Auto (Chetak), and Revolt Motors has led to the development of chargers with diverse power ratings. Typically, portable home chargers have operating power range from 250 W to 1.2 kW, featuring output voltages between 48 V and 72 V DC and charging currents ranging from 6 A to 15 A. These chargers generally complete the charging process within 4–6 hours [4]–[8]. Given the diversity of battery specifications and operating conditions, such charging systems must ensure adaptability, operational safety, and reliable performance.

Switching-mode power converters form the core of EV battery charging systems. Numerous isolated and non-isolated DC–DC converter topologies have been reported in the literature for EV charging applications [9].

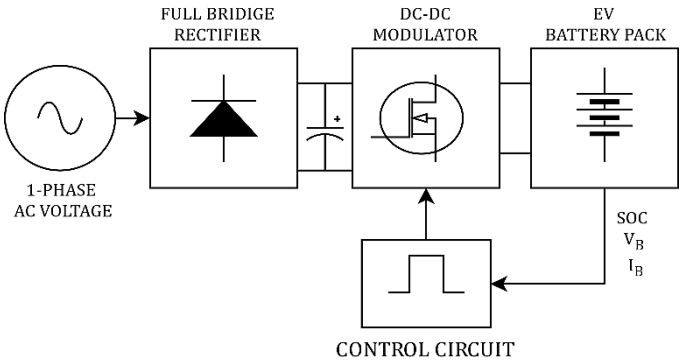

Figure 1. Block Diagram of an AC–DC EV Battery Charging System with Closed-Loop Control

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Figure 1 illustrates block diagram of an AC–DC EV battery charging system with the close loop control. In this system, single-phase AC supply is rectified and filtered using a full-bridge diode rectifier and a capacitor filter. The DC voltage is subsequently processed by a switching-mode DC–DC converter to deliver the voltage and current levels required for battery charging. Output regulation is achieved through closed-loop control, where feedback signals are used to adjust the pulse width of the converter switching signals.

Since the DC–DC converter determines the battery charging behaviour, converter selection requires major attention. Factors such as power level, efficiency, cost and isolation requirements govern the choice between isolated and non-isolated converter topologies. Non-isolated converters, including Buck, Boost, SEPIC, and Cuk configurations, are relatively simple and cost-effective. When Boost and Cuk converters are used with maximum power point tracking (MPPT), Boost converters work best when the source and load resistances are well matched. On the other hand, Cuk converters deliver stable power even when the operating conditions change [10]– [11]. However, the absence of galvanic isolation makes them unsuitable for off-board EV charging applications.

Isolated converter topologies such as flyback and forward converters offer galvanic isolation but are typically limited to power levels below 300 W due to increase in transformer stress and reduced in efficiency at higher power levels [12]–[13]. Recent improvements in snubber circuit design for flyback converters have demonstrated reduced voltage stress and switching losses leading to enhanced efficiency and reliability in low-power isolated applications [14].

To overcome these limitations, various hybrid converter configurations—such as SEPIC–Flyback [15],[16] and Forward–Flyback [17] have been proposed for higher voltage gain and improved efficiency with compactness. To enable bidirectional power transfer and flexible voltage conversion, some hybrid topologies including Flyback–Ćuk [18] and Ćuk–SEPIC [19] combinations, have been proposed. Even with significant improvements, these hybrid topologies frequently have heightened circuit complexity, elevated conduction losses, and inadequate scalability.

Recent studies indicate that phase-shifted full-bridge (PSFB) converters are well suited for EV charging applications due to their high efficiency and capability to achieve zero-voltage switching (ZVS). Although predictive current-mode control can enhance transient response, it introduces considerable computational complexity, which restricts its practical implementation on real-time platforms like dSPACE DS1104 [20]. Active-clamp circuits can improve energy recovery and reduce switching stress; however, they add complexity to the circuit design [21]. Hardware-tested PSFB converters demonstrated precise control and promising performance for charging low-voltage EV batteries [22], as they rely on advanced control techniques. Research on model predictive control (MPC) for DC–DC converters indicate enhanced transient performance and less overshoot relative to traditional PID-based control in constant load scenarios, underscoring the promise of predictive methodologies in power electronics [23].

To further enhance converter efficiency and reduce electromagnetic interference (EMI), various soft-switching techniques such as ZVS and zero-voltage zero-current switching (ZVZCS) have been introduced. For instance, an upgraded ZCZVT-PWM DC–DC boost converter with an active snubber cell showed zero-voltage and zero-current transitions, which led to less EMI, less switching stress, and better efficiency over a wide range of loads [24]. Advanced modulation strategies, including asymmetric PWM, adaptive control, and hybrid switching, have been shown to significantly reduce power losses [25]– [28]. However, their practical implementation often demands additional hardware and high-speed control algorithms, making them difficult to realize on real-time platforms such as the dSPACE DS1104 due to limited computational resources.

In addition to EMI and switching stress, EV chargers must safely withstand abnormal grid and load conditions. Studies on solid-state fault current limiters (SSFCLs) show that protection based on resonant circuits can efficiently limit fault currents and protect downstream components without causing major losses during normal operation. For example, a single-phase SSFCL prototype rated at 480 V and 16 A cut a peak fault current from 58.5 A to about 9 A. This was shown by MATLAB/Simulink simulations and real-world tests [29]. Such studies underscore the growing importance of fault-tolerant design considerations in EV charging systems.

To address the challenges with implementation simplicity, the present work proposes a conventional isolated full-bridge DC–DC converter directly fed from a diode-rectified single-phase AC source. The converter is made to give a steady output of 56 V at 15 A, which is suitable for charging EV batteries. A simple input capacitor is employed to suppress EMI and high-frequency switching transients, thereby reducing electromagnetic noise without increasing circuit or control complexity. The control scheme, comprising PWM generation and closed-loop voltage regulation implemented using the dSPACE DS1104 real-time controller [30]. The platform enables reliable real-time operation and high-resolution PWM generation. It also provides real-time observability, making it particularly suitable for rapid prototyping and experimental validation of EV charger power stages.

Table 1 presents a comparative analysis of the proposed full-bridge EV charger with representative full-bridge-based charger implementations reported in the literature.

The comparison highlights key aspects such as converter topology, control strategy, power level, experimental validation, and EMI/EMC considerations. By explicitly outlining both advantages and limitations, *table1* clarifies the design trade-offs and positions the proposed work within the context of existing full-bridge EV charging solutions.

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Table 1. Comparison of Existing Full-Bridge EV Chargers and the Proposed System

Parameter	LLC FB EV Charger [37]	Hybrid SSFB [38]	Conventional FB [39]	Proposed Work
Topology	LLC Full-Bridge	Hybrid Soft Switching FB	Conventional FB	Conventional Isolated FB
Control Strategy	Frequency modulation	Duty / auxiliary control	Phase-shift control	PI control (dSPACE DS1104)
Switching Method	ZVS/ZCS	Full soft-switching	Hard switching	Hard switching
Power Level	Medium–High (2–5 kW)	High (≈ 10 kW)	Medium (≈ 500 W–2 kW)	840 W
Experimental Validation	Simulation only	Hardware prototype	Simulation only	Hardware prototype
EMI Handling	Not discussed	Indirect (soft switching)	Not discussed	Measured spike reduction
EMI Mitigation Method	Topology-based	Auxiliary circuitry	Not addressed	Input capacitor + RC snubber
EMC Compliance	Not reported	Not reported	Not reported	Not evaluated (future work)
Key Advantage	High efficiency	High-power capability	Simple structure	Simple control, real-time validation
Key Limitation	Complex design	High circuit complexity	No experimental proof	No PFC; time-domain EMI only

2. PROPOSED CHARGER ARCHITECTURE

The proposed electric vehicle (EV) battery charger is designed to charge a 48 V, 25 Ah lithium-ion battery pack using a digitally controlled, closed-loop isolated full-bridge DC–DC converter. Block diagram of the Proposed Closed-Loop Full-Bridge EV Battery Charger with dSPACE1104 Control is shown *figure 2*. The complete power and control system is implemented with dSPACE DS1104 real-time controller. The architecture integrates the high-frequency isolated power stage, sensing circuits, and digital control algorithms on a unified real-time platform, enabling stable voltage regulation and flexible experimental evaluation of EV charging operation.

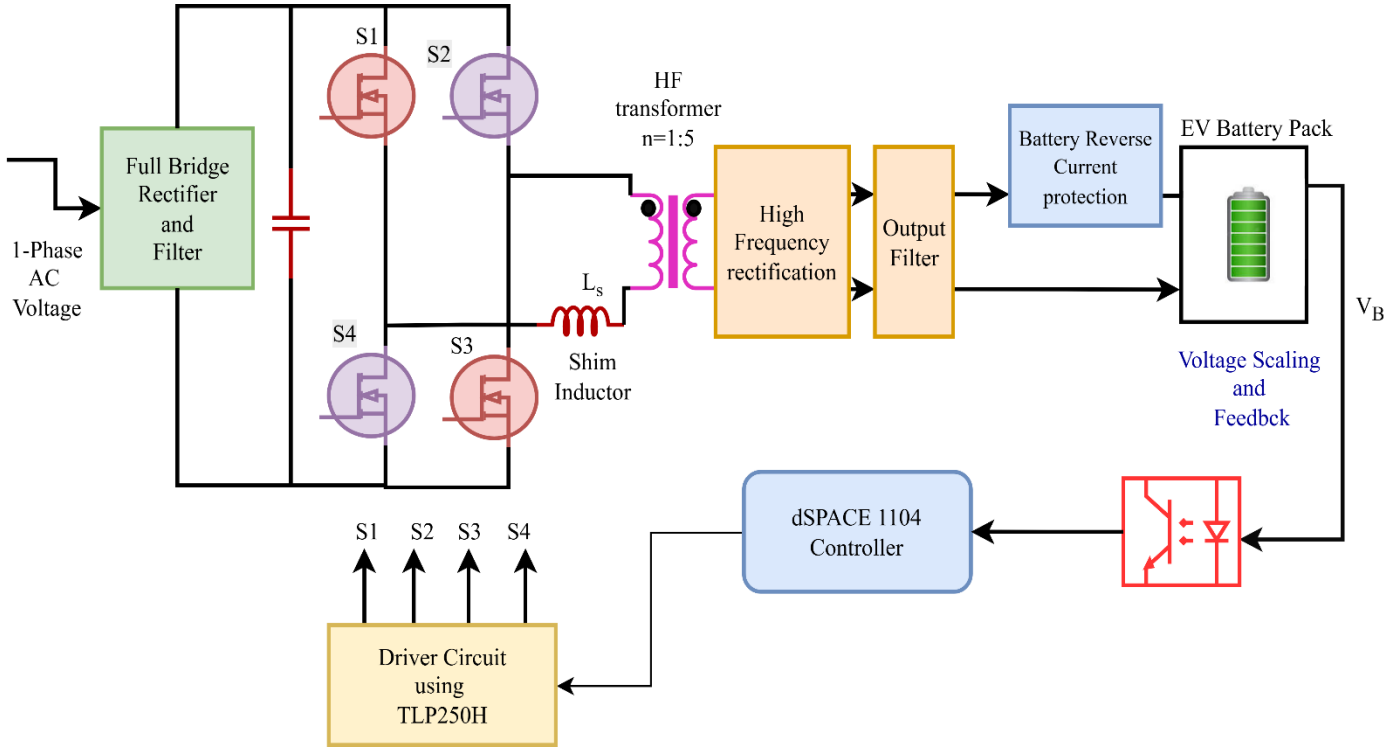

Figure 2. Block Diagram of the Proposed Closed-Loop Full-Bridge EV Battery Charger with dSPACE1104 Control

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The charger is supplied from a single phase 230 V ± 10%, 50Hz AC supply source. The input AC voltage is rectified using a diode bridge rectifier to obtain an unregulated DC voltage output, which is smoothed using a bulk DC-link capacitor to reduce low-frequency ripple and attenuate high-frequency switching noise before feeding the full-bridge DC–DC converter. The isolated full-bridge stage operates at a high switching frequency and excites a high-frequency transformer, which provides both galvanic isolation and voltage scaling. On the secondary side, a high-frequency full-bridge diode rectifier followed by an LC output filter generates a regulated low-voltage DC output suitable for EV battery charging. Output regulation is performed through closed-loop digital control, in which the output voltage is sensed and fed back to the controller via signal-conditioning and opto-isolation circuits to maintain safe electrical separation between the power and control stages. The conditioned feedback signals are then sampled in real time using the analog-to-digital converter (ADC) channels of the dSPACE DS1104 platform. In the MATLAB/Simulink environment, the measured output voltage is compared with a reference setpoint and the resulting error is processed using a proportional–integral (PI) controller. The PI gains were selected using a practical, experiment setpoint, tuning approach, where gains were iteratively adjusted. The controller tuning approach adopted in this work follows practical industrial methods commonly used during the initial stage of hardware prototyping. Experimental observations showed that the closed-loop system operated stably under all tested operating conditions. No oscillatory behavior was observed, even during sudden load variations, confirming the reliability of the control strategy. The experimentally observed stable response under steady-state and load-transition conditions is considered sufficient for proof-of-concept real-time validation, while formal small-signal stability analysis is identified as future work. The voltage control loop of the proposed full-bridge DC–DC converter is implemented using a PI controller on the dSPACE DS1104 platform. The critical gain was determined using MATLAB/Simulink by gradually increasing the proportional gain until sustained oscillations occurred, resulting in a critical gain (Kcr) of 0.32. Based on this value, the PI controller parameters were selected as Kp = 0.144 and Ki = 17.68 to achieve stable operation along with a satisfactory transient response. The control algorithm generates the required pulse-width-modulated (PWM) gating signals, which are applied to the full-bridge switches via the dSPACE controller. Each power switch (MOSFET/IGBT) in the full-bridge is driven through an isolated gate driver stage based on the TLP250H. The gate driver provides level shifting, galvanic isolation and sufficient drive capability to ensure fast and reliable switching of the four power devices. Switches S1 and S3 are operated simultaneously, while switches S2 and S4 are driven in the complementary interval. Adequate dead-time is incorporated between complementary switch transitions to prevent shoot-through across the DC bus and ensure safe converter operation.

3. Prototype Design and Implementation

This section outlines the realization of the proposed EV battery charger at the hardware level. The system consists of an AC–DC rectification stage followed by a high-frequency isolated full-bridge DC–DC converter. Design aspects such as device selection, transformer configuration, and gate-drive circuitry are addressed. All design parameters are obtained through analytical calculations and are suitable for real-time operation with the dSPACE DS1104 controller, enabling consistent experimental verification.

The closed-loop control scheme used in the charger is shown in *figure 2*. The key electrical ratings of the proposed charger, derived from the selected power devices, transformer design, and output filter, are summarized in *table 2*.

Table 2. Specification of proposed EV charger

Parameter	Specification
Input AC Voltage (V_{ac})	230 V±15%
Rectified DC Voltage ($V_{DC(nom)}$)	325 V DC
Switching Frequency (f_s)	50 kHz
Output Voltage (V_o)	56 V DC
Maximum Output Power (P_o)	840 Watt

3.1. Power Stage Design

The charger incorporates a two-stage conversion structure which includes an AC–DC rectifier with a capacitor filter and a high-frequency isolated full-bridge DC–DC converter The power components are designed to supply up to 840 W at 56 V with a maximum output current of 15 A. The design methodology for each stage is discussed in the subsequent sections.

3.1.1. AC–DC Rectifier Design

The single-phase AC supply of 230Vrms±15% is processed by a diode full-bridge rectifier. The nominal rectified DC voltage is given by:

$$V_{DC(nom)} > \sqrt{2} * V_{ac(max)} > 325V \quad (1)$$

The output power of the charger is designed for 840 W. Assuming an efficiency of 80% for the full-bridge DC–DC converter, the input power (Pin) to the converter is calculated as:

$$P_{in} = \frac{P_o}{\eta} = 1050W \quad (2)$$

Where, *Po* is the output power and η is the converter efficiency.

This input power to the full-bridge converter is provided by the output of the front-end AC-DC rectifier. Assuming a power factor of 0.7, the real input power drawn from the AC mains becomes:

$$P_{AC} = \frac{P_{in}}{p.f} = 1500W \quad (3)$$

3.1.2. Selection of DC-Link Voltage and Capacitor

The maximum DC link voltage for single phase EV charger is 375V. The maximum input current ($I_{in(max)}$) occurs at the

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minimum input line voltage ($V_{DC(min)}$) with the maximum output Power. The minimum DC link voltage in case of single-phase EV charger is given by:

$$V_{DC(min)} > \sqrt{2} * V_{ac(min)} > \sqrt{2} * 195 > 275V \quad (4)$$

The maximum input current to the full-bridge DC–DC converter occurs at the minimum DC link voltage:

$$I_{IN(max)} = \frac{P_{in}}{V_{DC(min)}} = \frac{1050}{275} = 3.82A \quad (5)$$

Assuming that the percentage of non-conducting period is minimal, the required output capacitor of rectifier can be calculated as shown in *eq. (6)*

$$C_{DC(link)} = \frac{2 * P_{in}}{\pi \times V_{DC(min)} \times \Delta V_{DC(min)} \times f_{line}} = 1768\mu F \quad (6)$$

The Standard capacitor of 1800uF is used for the design of hardware prototype.

3.1.3. Input AC Current calculation

The peak input current calculated with minimum AC voltage is:

$$I_{AC(max)} = \frac{P_{AC}}{V_{AC(min)}} = 7.69A \quad (7)$$

3.1.4. Diode selection

The reverse voltage rating of the rectifier diodes must exceed the peak input AC voltage calculated as

$$V_R = \sqrt{2} * V_{ac(max)} = \sqrt{2} * 265 = 375V \quad (8)$$

By considering safety margin of 1.5 , the reverse voltage is calculated as

$$V_R = 1.5 * \sqrt{2} * V_{ac(max)} = 562.5V \quad (9)$$

A suitable general-purpose diode for this design is the 10A10, with a reverse voltage rating of 1000 V and current capability of 10 A used in the experimentation.

3.2. Design of full bridge DC-DC converter

The design process for FB DC-DC converter is explained in detail below.

3.2.1. High frequency Transformer Design

For designing a high frequency transformer, power capacity, selection of ferrite core, turns ratio, number of primary and secondary turns and calculation of winding wire size are required [32]:

(a) Transformer turns ratio

The basic output voltage equation for the transformer is given by

$$V_o = V_{DC(min)} \times \frac{N_S}{N_P} \times 2 \times \frac{t_{on}}{T} \quad (10)$$

From *eq. (10)*, the transformer turns ratio calculated as,

$$n = \frac{N_S}{N_P} = \frac{V_o}{2 \times V_{DC(min)} \times \frac{t_{on}}{T}} = 0.255 \quad (11)$$

(b) Ferrite Core Selection

The selection of core is based on the area product. The core area product is calculated as,

$$A_P = \frac{P_O \times D_{cma}}{0.0014 \times B_{MAX} \times f_s} = 3.75cm^4 \quad (12)$$

Where, Bmax=1600G, fs=50kHz, D_{cma} =500 circular-mills

From the design calculations, the minimum required AP was found as 3.75cm^4. A ferrite core of type E55/28/21 (TDK, part number B66335) selected, offering an AP of 6.782 cm^4 (with effective core area of 3.54cm^{2}and window area of 1.87cm^2 which meets the design margin. The core dimensions provided by the manufacturer are shown in *figure 3*, which serve as the basis for winding arrangement, insulation clearance, and thermal considerations [31].

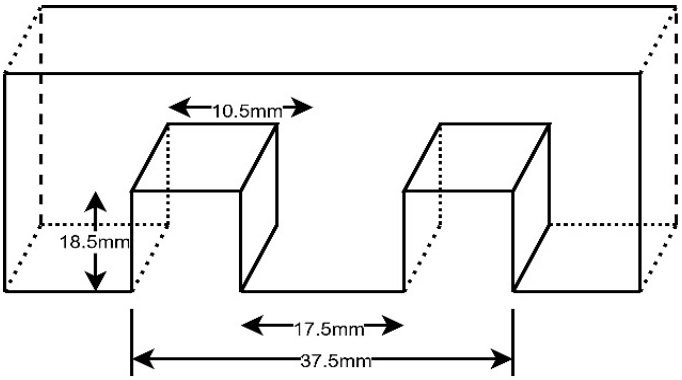

Figure 3. Dimensions of the E55/28/21 ferrite core (TDK B66335)

(c) Number of Turns

After selection of the core, the number of Primary turns (N_P) and Secondary turns (N_S) are calculated as follows,

$$N_P = \frac{(V_{dc}min - 1)(0.8T/2)}{A_e \times dB} = 20 \quad (13)$$

$$N_S = n \times N_P \approx 5 \quad (14)$$

(d) Winding wire size

The equivalent primary flat-topped current Ipft is calculated by

$$I_{pft} = \frac{1.56 \times P_O}{V_{dc}} = 5.95 \quad (15)$$

(i) Primary Wire Size Selection: Current I_{pft} flows at a duty cycle of 0.8 so its RMS value is calculated as follows,

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$$I_{RMS} = I_{pft\times\sqrt{0.8}} = 5.32A \quad (16)$$

At a current density of 500 circular mils per RMS ampere, the required number of circular mils calculated as follows,

$$Number\ of\ Circular\ mils\ = \frac{500 \times 1.40 \times P_O}{V_{dc}} = 2 \quad (17)$$

From the SWG selection table, 16-gauge wire is used for primary winding.

(ii) Secondary Wire Size Selection: RMS current in each half secondary is calculated as,

$$I_{SRMS} = I_{DC} \times \sqrt{D} = 9.48A \quad (18)$$

At 500 circular mils per rms ampere, the required number of circular mils for each half secondary is

$$Number\ of\ Circular\ mils\ = 500 \times I_{SRMS} = 474 \quad (19)$$

From the SWG table, 13-gauge wire is used for the secondary winding.

3.2.2. Selection of semiconductor devices

(a) Selection of Current and Voltage rating (Primary Side)

The maximum input current as per *equation (5)* for the full-bridge DC–DC converter is 3.82A. Since the full-bridge topology splits the load current between two devices in each conduction cycle, each primary switch must handle approximately half of the maximum input current. So, the current rating of each switch is 2.85A with safety margin of 1.5. Voltage rating ($V_{DS(rated)}$) is calculated as:

$$V_{DS(rated)} = 1.5 * V_{DC(max)} = 562V \quad (20)$$

An 12n65 MOSFET is selected which offers a maximum voltage and maximum current rating of 650V and 12A respectively for the converter.

(b) Selection of Current and Voltage rating (Secondary Side)

A high frequency full bridge rectifier was used at secondary side. Two diagonal switches conduct at same time. The secondary rms current (I_{SRMS}) derived in equation 19 is 9.48A. With safety factor of 1.5, secondary diode should have maximum current rating of 14.22A. During inverse voltage blocking secondary side diode have twice the secondary peak voltage as calculated by:

$$V_{s(peak)} = 2 \times V_{DC(max)} \times n \times D = 56V \quad (21)$$

An ultrafast recovery diode FML33S is selected, which has maximum peak inverse voltage and maximum average rectified current rating of 400V and 20A respectively.

3.2.3. Control circuit, Gate-Driver Arrangement and Dead-Time

The on-board slave DSP of dSPACE-1104 platform was used to generate gate pulses of 50kHz for FB DC-DC converter. As per [32], two MOSFETs on same leg should not be turned on simultaneously to prevent short across supply terminals. To ensure this, maximum duty cycle for each switch was 0.4. Therefore, duty cycle of the gate pulses generated with dead time of 2µs with 50kHz switching frequency. The TLP250 high-speed, high isolation photocoupler is used for driving MOSFET. The TLP250H provides 500 ns propagation delay, ensuring safe operation at the 50 kHz switching frequency. In the prototype design four individual driver sections are prepared. The TLP250H is supplied from isolated linear regulator of 12V.At the output pin 6, a series resistor and 10k pull down resistor are connected to prevent false turn-on and controlling switching speed.

For closed-loop control and real-time feedback, output voltage and current sensing circuits were incorporated. The converter output voltage of 56 V was scaled down to 3.3V using a resistive voltage divider and electrically isolated using a PC817 opto-coupler before being applied to the ADC input of the dSPACE DS1104. This isolation ensures safe signal conditioning and protects the DSP from high-voltage disturbances.

Dead-Time Calculation

As per reference [33], the minimum dead time is calculated by:

$$t_{dead}\ = \left(t_{td\_off}^{max} - t_{d\_on}^{min}\right) + 1.2(t_{pdd}^{max} - t_{pdd}^{min}) \quad (22)$$

where $t_{d_off}^{\max}$and $t_{d_on}^{\min}$are the MOSFET turn-off and turn-on delays, and $t_{pdd}^{\max}$and $t_{pdd}^{\min}$represent the propagation delay spread of the gate driver.

Using references [34] and [35]

$(t_{d\_off}^{\max} \approx 200\ \text{ns}, t_{d\_on}^{\min} \approx 30\ \text{ns})$

$(t_{pdd}^{\max} \approx 500\ \text{ns}, t_{pdd}^{\min} \approx 150\ \text{ns})$,

equation (22) gives

$$t_{\text{dead}} = (200 - 30)\ \text{ns} + 1.2(500 - 150)\ \text{ns} = 590\ \text{ns} \quad (23)$$

To provide a safety margin to avoid shoot-through under worst-case conditions for the experimentation, a dead time 2µs is implemented in the prototype nearer to calculated deadtime of 590ns.

3.2.4. Output inductor (L_O) and Output Capacitor (C_O)

$$L_o\ = \frac{(0.5 - D) \times V_o \times T}{\Delta I_L} = 373\mu H \quad (24)$$

$$C_o\ = \frac{(D) \times I_o \times T}{\Delta V_o} = 214\mu F \quad (25)$$

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3.2.5. Design of RC Snubber Circuit

RC snubber circuit was designed based on the leakage inductance of the high-frequency transformer and ringing frequency [36]. The resistor and capacitor for the snubber circuit is calculated as per *equation (26) & (27)*. *Figure 4* shows measurement of the leakage inductance, 172uH on LCR meter and *figure 5* represents ringing waveform across the MOSFET on DSO during switching transitions. The measured ringing frequency without any snubber circuit was 7.143 MHz.

$$C_p = \frac{1}{(2\pi f_r)^2 \times L_{lkg}} = \frac{1}{(2\pi \times 7.143M)^2 \times 172\mu} = 2.8pF \quad (26)$$

$$R_s = \sqrt{\frac{L_{lkg}}{C_p}} = 7.9k\Omega \quad (27)$$

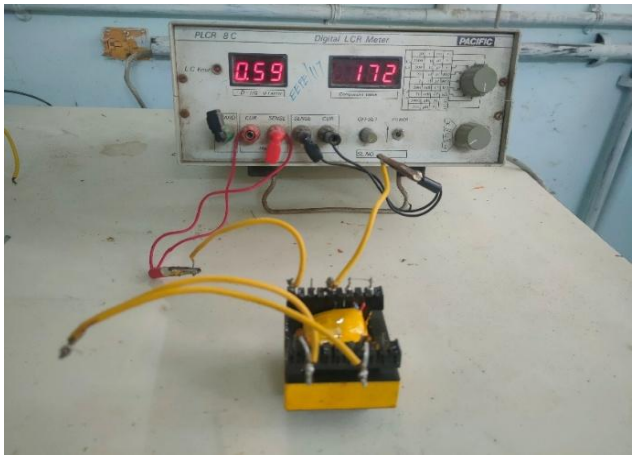

Figure 4. LCR meter reading of leakage inductance

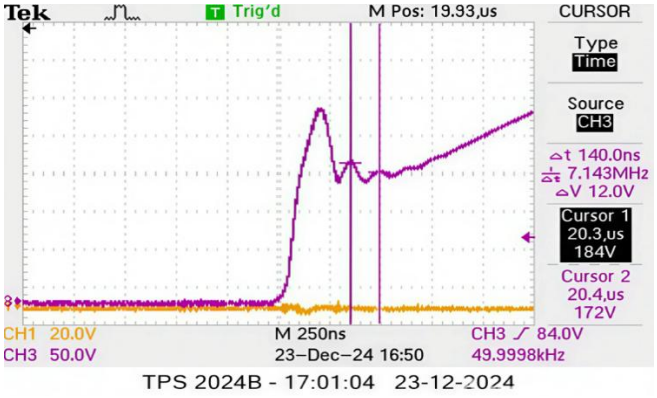

Figure 5. Ringing waveform across MOSFET during switching transitions

4. SIMULATION AND EXPERIMENTAL RESULTS & DISCUSSION

This section validates the proposed closed-loop full-bridge EV battery charger through simulation and hardware experiments. The work also includes its hardware prototype design, verification of gate-drive signals, and analysis of its output voltage and current waveforms. Switching stress, EMI performance, and efficiency are evaluated under practical operating conditions.

The results confirm the correctness of the proposed design methodology and demonstrate reliable real-time operation using the dSPACE DS1104 controller. All experimental results reported in this study correspond to partial-load operation due to laboratory power and load constraints, while the hardware and control design are rated and analytically validated for the full 56 V, 15 A operating condition. The closed-loop full-bridge battery charger was first modelled in MATLAB/Simulink using the parameters calculated in the design section. practically hardware prototype was developed and experimentally implemented using the dSPACE DS1104 real-time controller to validate the simulation results. A 48 V, 25 Ah lithium-ion battery pack was used for experimental testing. The electrical specifications of the proposed EV charger and the hardware specifications used for experimentation are presented in *table 2* and *table 3*, respectively.

Table 3. Hardware Specifications

Parameter	Specification
Rectifier filter capacitor	1800uF
Transformer Turns Ratio (N_P:N_S)	5:1
Output Filter Inductor	250uH
Output Filter Capacitor	330uF

4.1. Hardware Prototype Setup

Experimental hardware setup of the proposed closed-loop full-bridge EV battery charger is shown in *figure 6* with the design specification as per *table 2*. The system includes a full-bridge AC–DC rectifier, high-frequency isolated DC–DC converter, dSPACE1104 real-time control unit, and a 48 V, 25 Ah lithium-ion battery. All measurements conducted using a digital storage oscilloscope (DSO) with isolated probes in the high-voltage experimentations.

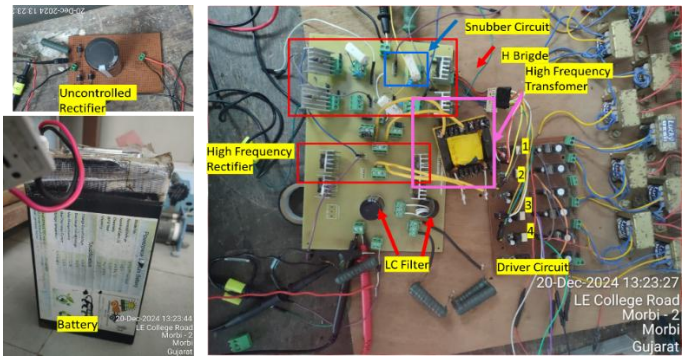

Figure 6. Experimental hardware setup of the proposed closed-loop full-bridge EV battery charger

4.2. Gate pulses

The dSPACE1104 controller was programmed in MATLAB/Simulink to generate gate pulses for the MOSFETs of the full-bridge converter. A sufficient dead time inserted to avoid shoot-through. *Figure 7(a)* shows the simulated gate pulses for switches S1–S4 and *figure 7(b)* shows the gate pulses captured from the gate driver outputs using an oscilloscope from the prototype hardware of the proposed EV charger. The

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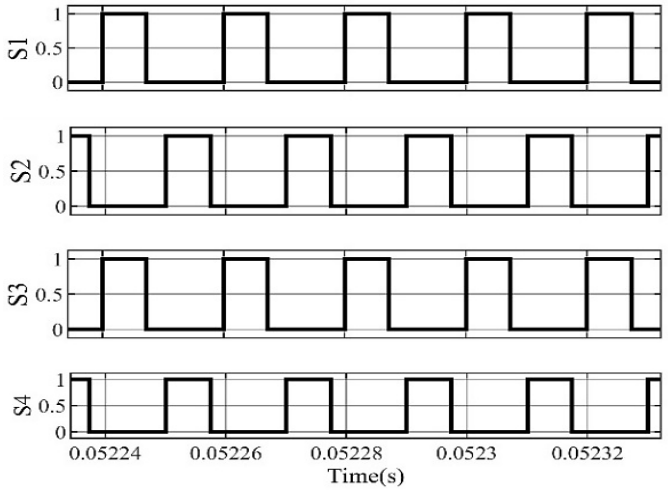
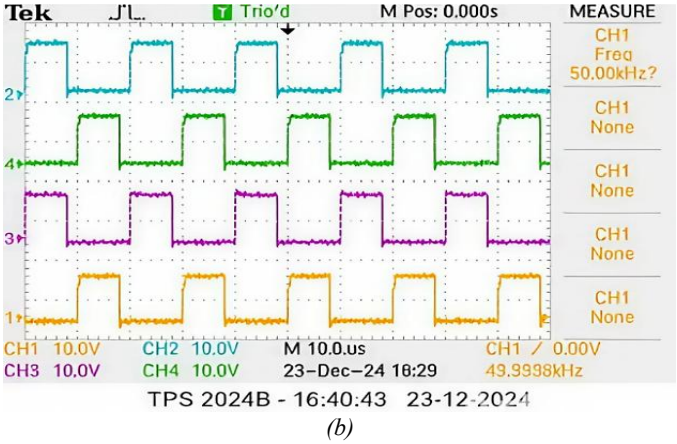
experimental pulses closely match the simulation in terms of duty cycle, frequency, and dead time.



(a)

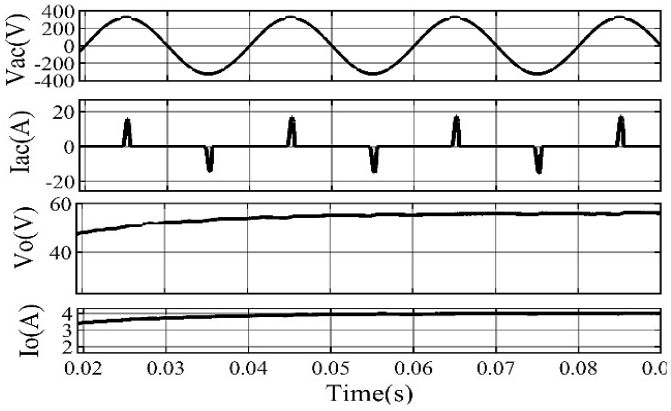


(b)

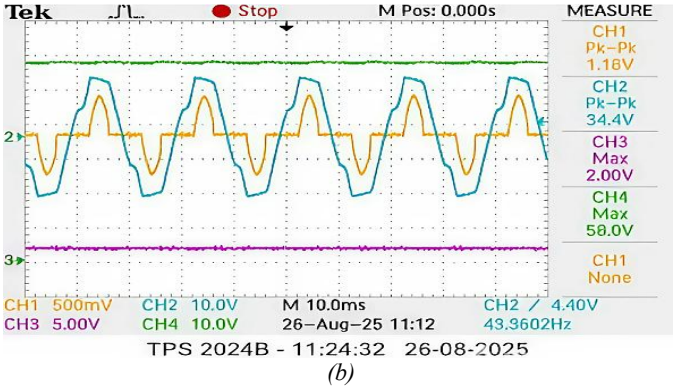
Figure 7. *(a)* Simulated gate pulses for switches S1–S4.; *(b)* Hardware gate pulses measured at the TLP250H driver outputs

4.3. Output Voltage and Current waveforms

The charger output voltage and current waveforms captured for both simulation and hardware prototypes. *Figure 8(a)* shows the simulated input and output current and voltage waveforms and *figure 8(b)* shows input and output current and voltage waveforms of hardware prototype.



(a)

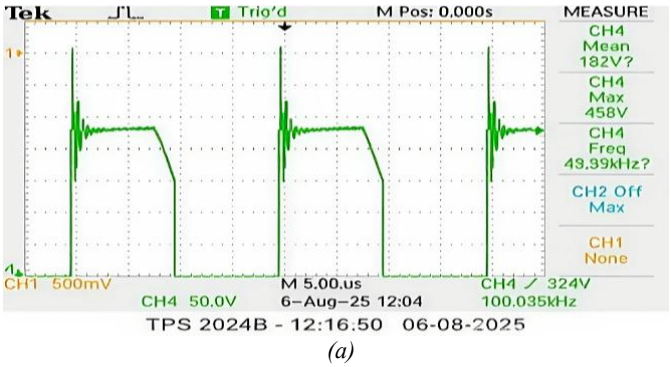


(b)

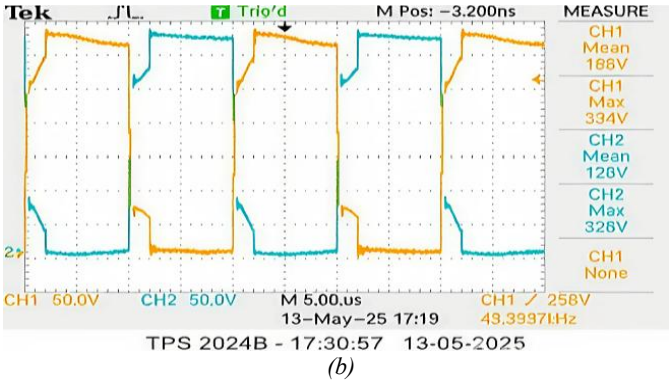
Figure 8.: *(a)* simulated input and output waveforms of current and voltage *(b)* input and output waveforms for current and voltage for hardware prototype

4.4. Mitigation of Switching Spikes and Ringing

During testing, high-frequency spikes and ringing were observed across the MOSFETs as shown in *figure 9(a)*. Electromagnetic interference (EMI) effects were observed due to the use of jumper wires; discrete component leads and unavoidable parasitic inductances in the experimental setup. At 230 Vac, the maximum voltage stress across the switch was 458 V without any suppression capacitor. To suppress this, capacitor placed at the input of the full-bridge, which significantly reduces the transient spikes and high-frequency oscillations to 330V as shown in *figure 9(b)*. It is important to note that the proposed work does not claim compliance with EMC standards. Formal conducted and radiated EMI measurements in accordance with CISPR/IEC standards are beyond the scope of this study and are identified as future work.



(a)



(b)

Figure 9. (a) MOSFET voltage stress waveform without capacitor (b) MOSFET voltage stress waveform with capacitor for 2A load current

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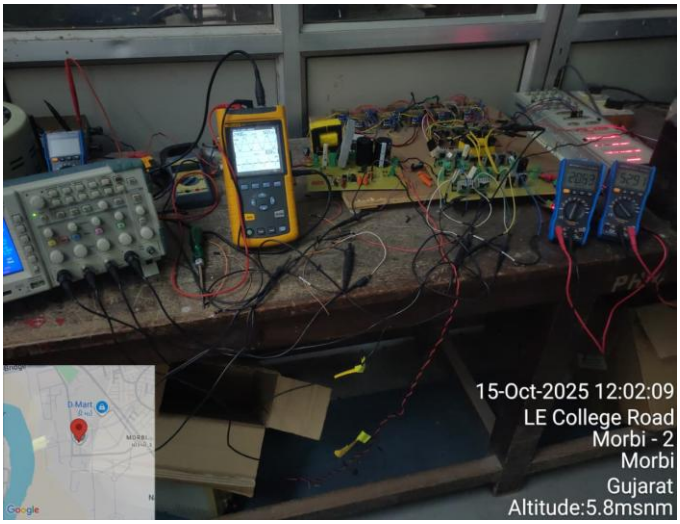
4.5. Efficiency Calculation

The efficiency is calculated based on the operating point measured in digital multimeter and power analyzer. *Figure 10(a)* shows the measurement of output voltage and current waveforms and *figure 10(b)* the measured power factor and input power from the AC side on the hardware prototype. The proposed charger tested under a typical working condition, the output voltage 52.91 V and the current 2 A, giving an output power of about 106 W and the input side, the power analyzer showed 1.13 kW, but this was a scaled reading because of the gain settings in the measurement system. The actual input power was 0.113 kW (113 W). The efficiency is calculated as

$$\eta = \frac{P_{OUT}}{P_{IN}} = 92\% \quad (28)$$

These results show that the converter works efficiently even when it is not running at full capacity.



(a)

(b)

Figure 10. *(a)* Output voltage and current waveforms on hardware prototype *(b)* Power factor and input power on hardware prototype

5. CONCLUSION

This design, real-time implementation, and experimental validation of a medium-power isolated full-bridge DC–DC converter-based EV battery charger using the dSPACE DS1104 rapid prototyping platform presented in this paper. A complete, calculation-driven development methodology was demonstrated, including front-end AC–DC rectification, full-bridge DC–DC conversion, high-frequency transformer design, sensing isolation, dead-time implementation, and closed-loop PI control. The proposed architecture provides galvanic isolation and stable voltage regulation, making it suitable for research-oriented EV charger prototyping and experimental investigations.

Experimental results confirm reliable real-time operation of the prototype, delivering a regulated output voltage in the range of 48–56 V. A simple passive EMI mitigation approach employing an input capacitor and RC snubber was experimentally validated, resulting in a significant reduction in MOSFET voltage stress from 458 V to 330 V and effective suppression of high-frequency ringing. The converter achieved an efficiency of approximately 92% under partial-load operation, validating the correctness of the power-stage design and real-time control implementation. The primary contribution of this work lies in the system-level integration and real-time experimental validation of a full-bridge EV charger, demonstrating a transparent and reproducible design and implementation framework suitable for academic research and early-stage development. The experimental results establish a solid foundation for further performance enhancement and functional expansion. Building on this validated platform, future work will focus on full-load efficiency characterization, detailed loss analysis, implementation of closed-loop CC–CV battery charging operation and comprehensive EMC evaluation to extend the applicability of the proposed system toward more advanced EV charging scenarios.

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