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Design of a High Frequency DC-DC Converter with a Bootstrap MOSFET Driver Circuit

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ABSTRACT- The development and improved accessibility of modern microchips and semiconductor components enable the design of more cost-effective and efficient high-frequency converters. The selection of the power circuit topology and control system, which directly influence device performance, is of critical importance when designing a high-frequency converter. Among the primary elements of the control system are transistor drivers, with the bootstrap driver implementation gaining particular popularity due to the proliferation of single-package isolated high-side and low-side switch ICs. The application of this driver circuitry in a 100 kHz PSFB DC-DC converter presents several limitations and specific characteristics that are examined in detail in this study. This work provides experimental results (oscillograms) from testing a developed 3 kW PSFB DC-DC converter with bootstrap transistor drivers operating under a load consisting of a secondary H-bridge DC-AC converter. The incorporation of AND logic gate ICs into the control signal paths of high-side transistor drivers to provide additional hardware protection against malfunctions during microcontroller loading/failure/reboot conditions introduces a control signal delay of approximately 5 ns, representing less than 1% of the PWM period, yet sufficient to cause asymmetric power transformer currents and subsequent magnetic saturation. The research findings may be valuable and applicable for designing similar types of power conversion systems.

Keywords: Bootstrap MOSFET Driver, PSFB DC/DC, PWM, High Frequency, Asymmetrical, Saturation Current.

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1. INTRODUCTION

The development and growing demand for alternative energy sources, particularly photovoltaic solar panels designed for individual use with power outputs of up to several kilowatts, necessitates the construction of systems that convert direct current (DC) voltage into alternating current (AC) voltage to enable the connection of household electrical appliances [1-4]. In most cases, such a power supply system consists of a source (photovoltaic solar panels) connected to low-voltage energy storage units—battery packs—and a galvanically isolated DC/AC converter that generates an AC voltage with specified amplitude and frequency parameters [5]. One possible structure for this type of galvanically isolated converter can be implemented through double conversion: DC/DC and DC/AC [6-8]. Since the voltage of a low-voltage battery pack ranges from 24 V to 110 V depending on the battery type and configuration, the currents in the primary side of the DC/DC converter can reach hundreds of amperes. To ensure the safe operation of the entire device, especially its primary side, it is crucial to properly control the power transistors. The most common types of drivers used for transistor control are individual switch drivers with their own voltage sources or a bootstrapping driver circuit, which uses a single common voltage source [9]. It is important to note that earlier SiC and MOSFET transistors required a bipolar driving voltage (+20/–15 V to –3/–5 V), which necessitated the use of individual drivers with dedicated power supplies. Modern SiC and MOSFET transistors allow for unipolar driving (+15/0 V), making it possible to use a bootstrapping driver circuit. For example, bootstrapping driver circuits are used in nearly all modern application notes (such as AN145544, AN230508, AN_201710_PL52_001, ER_2102_PL52_2102_154546, AN_201609_PL52_004, and others) by "Infineon".

Moreover, as described above, the converter is connected to a source (battery pack) with a low voltage value and, consequently, a high current, which necessitates the use of a two-switch forward converter topology – specifically, a Full Bridge (Push-Pull and other topologies are not considered due to the limited window size of the planar power transformer implemented on an ER64/13/51 core).

Therefore, the aim of this research is to analyze the specifics of applying a bootstrap driver circuit in the developed 3 kW PSFB DC/DC converter [10-11].

2. BOOTSTRAP DRIVER

The main advantage of using a bootstrap driver circuit for the transistors is its simplicity and reduced component count, owing

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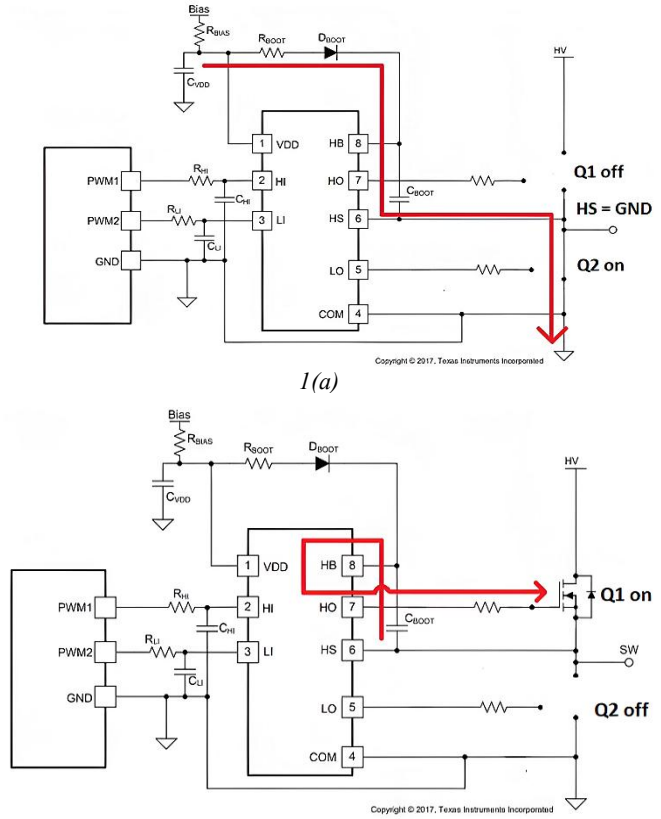
to the use of a common voltage source that provides the required level for proper transistor operation (turn-on). *Figure 1* demonstrates the operating principle of the bootstrap circuit using the example of one leg of the PSFB DC/DC converter [12].



1(a)

1(b)

Figure 1 (a), (b). Operating principal bootstrap driver [Source: Texas Interments Incorporated]

It is important to note that *figure 1* depicts a driver without galvanic isolation, as the ground (GND) of the logic control signals is connected to the negative bus of the power transistors. In the system under investigation, the digital and power circuits are galvanically isolated.

The charging of the capacitor CBOOT, which provides the supply voltage for the high-side driver, is accomplished by the current flowing through the low-side transistor Q2. Subsequently, Q2 is turned off, resulting in a potential across the capacitor CBOOT approximately equal to VBIAS, accounting for the voltage drop across RBOOT and DBOOT (approximately 0.6 V).

Based on the described operating principle, the bootstrap circuit has a number of features and limitations: the diode DBOOT must be rated for the maximum reverse voltage of the power circuits (taking into account switching voltage spikes); transistor Q2 must initially be turned on to charge the capacitance CBOOT; transistors Q1 and Q2 must operate in switching mode, and the maximum duty cycle must be strictly less than 100% to allow charging of the bootstrap capacitance.

The developed 3 kW PSFB DC/DC converter operating at 100 kHz utilizes the TMS320F28035 microcontroller, and the hardware configuration of the ePWM module is implemented in accordance with the "TMS320x2802x, 2803x Piccolo Enhanced Pulse Width Modulator (ePWM) Module" (*figure 2*), with the exception of the CMPB value.

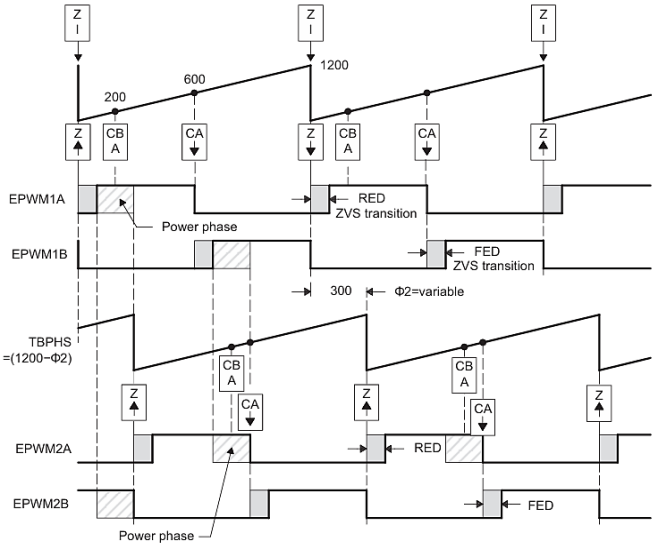


Figure 2. Hardware setup of ePWM module

The CMPB value is used as a flag event for ADC triggering and conversion, corresponding to 90% of the "Power phase" (*figure 2*) to measure the peak value of the transformer current while avoiding the digitization of incorrect values (noise) induced by switching transients. Since the duration of EPMW1A and EPWM2A is determined by the fixed CMPA value (according to *figure 2*, equal to 600, with a total period of 1200 – the example is given for a PWM frequency of 50 kHz, whereas the developed converter operates at a PWM frequency of 100 kHz) and utilizes dead-time generation in "Active High Complementary (ACH)" mode, the PWM is enabled after microcontroller initialization, with the first control signal applied to *Q1* according to *figure 1*, without the possibility of individually disabling the PWM signals for the high-side transistors. Initial activation of the high-side switch without a charged bootstrap capacitor (the voltage level depends on the circuit components' leakage current) leads to incomplete turn-on (opening) of the transistor, causing it to enter linear mode (high channel resistance), and subsequently, when the low-side switch is turned on, thermal runaway occurs, resulting in failure of the entire unit.

To reduce the microcontroller software overhead associated with additional initialization code and/or software-based disabling of PWM channels, as well as to incorporate hardware protection ensuring prevention of initial high-side switch activation, a circuit with an additional PWM enable signal was developed. This signal is implemented using the Nexperia 74HCT08D.653 (TTL) AND logic gate IC (*figure 3*).

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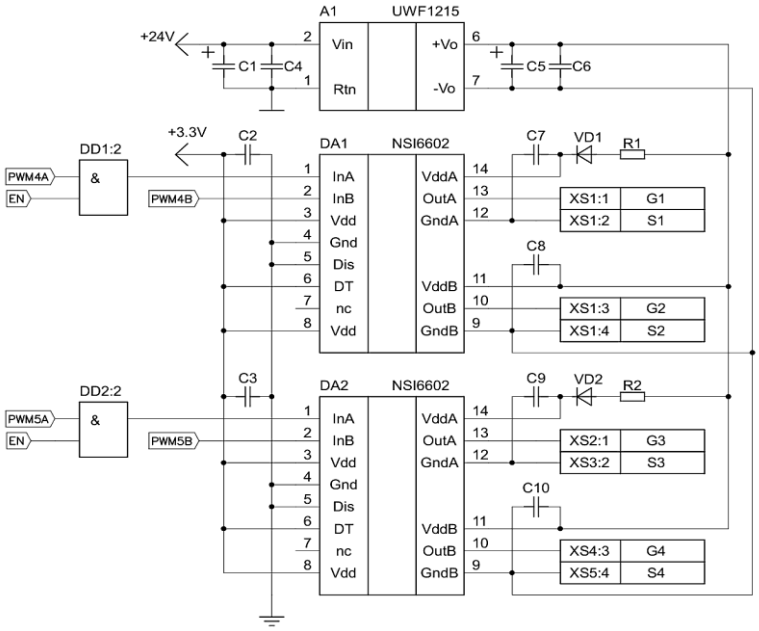

Figure 3. Driver circuit with enable signal

Thus, according to the circuit, the PWM signals continuously switch the lower transistors, which in turn charges the bootstrap capacitor. The enable signal ENABLE ("EN" *figure 3*) is generated by a GPIO I/O pin of the microcontroller when the converter transitions from standby mode to operation. This solution provides hardware protection against initial turn-on of the high-side transistor. The driver IC used is the NSI6602 in an SOW16 (SOIC16-300) package, providing an isolation voltage of 5700 VRMS. Another significant advantage of this IC is its high peak output current capability, which allows direct connection to transistors through a gate resistor (gate resistors are installed on the power board shown in *figure 5* in close proximity to the power transistors), and the ability to generate dead-time through an external resistor RDT.

Table 1. Components of the circuit in *figure 3*

Positional designation	Name	Description
A1	UWF1215S-3WR3	DC/DC CONVERTER 4.5-36/15V 3W SIP7
DA1, DA2	NSI6602B-DSWR	DGTL ISO 5.7KV DUAL GATE DRVR 16SOIC
DD1, DD2	74HCT08D.653	IC 4 2AND 2-6V SO14
C1, C5	TAJA225K035RNJ	CAP TANT 2.2UF 10% 35V 1206
C2, C3, C6	CC0805KKX7R9BB105	CAP CER 1UF 50V X7R 0805
C4, C7-C10	CL31B106KBHNNNE	CAP CER 10UF 50V X7R 1206
VD1, VD2	US1MF	DIODE UF 1000V 1A 35NS SOD123FL
R1, R2	RC1206FR-0715RL	RES SMD 15 OHM 1% 1/4W 1206
XS1, XS2	DS1015-04-06R6XT	CONN HEADER VERT 6POS 2.54MM

It is important to note that the developed driver with this IC is intended exclusively for controlling SiC and MOSFET transistors, as it lacks built-in soft-shutdown features that are necessary for safe shutdown of IGBTs during fault conditions, for example [13].

3. EXPERIMENTAL STUDY OF A PSFB CONVERTER PROTOTYPE

Figure 4 shows a prototype of the developed 3 kW PSFB DC/DC converter operating at a PWM frequency of 100 kHz and designed for a nominal input voltage of 110 V (the minimum possible input voltage is 65 V).

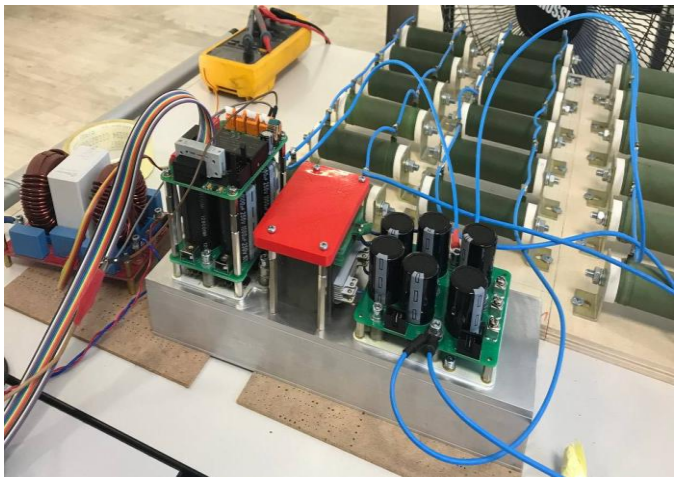

Figure 4. Prototype of a PSFB converter

The power stage utilizes pairs of Infineon IPB200N25N3 field-effect transistors with an on-state resistance of approximately 20 mΩ. *Figure 5* shows the schematic diagram of the primary power section, and *table 2* lists the components.

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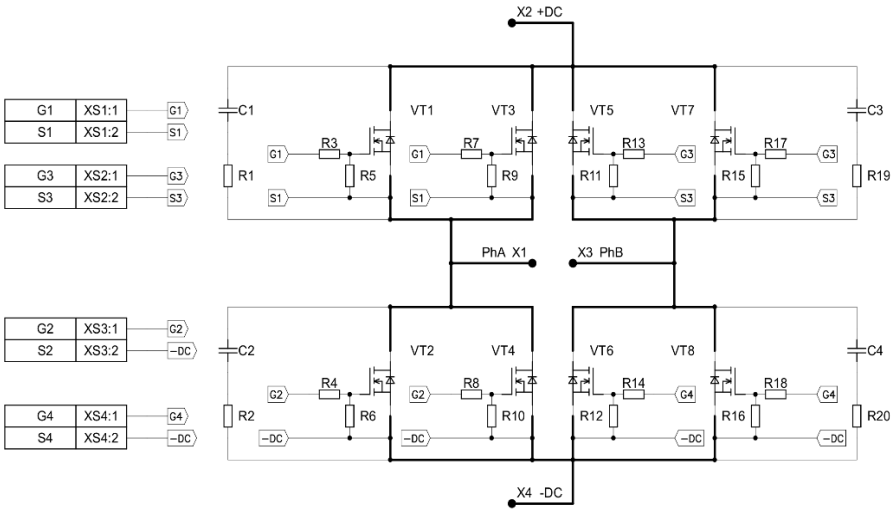

Figure 5. Schematic diagram of the primary power section of the PSFB DC/DC

Table 2. Components of the circuit in *figure 5*.

Positional designation	Name	Description
VT1-VT8	IPB200N25N3	MOSFET N-CH 250V 64A D2PAK
R5, R6, R9, R10, R11, R12, R15, R16	RC0603FR-0710KL	RES SMD 10K OHM 1/10W 0603
R3, R4, R7, R8, R13, R14, R17, R18	RC0805FR-0710RL	RES SMD 10 OHM 1/8W 0805
R1, R2, R19, R20	MCHP122WF150JT4E	RES SMD 15 OHM 1% 2W 2512
C1-C4	CC1206JKNPOCBN471	CAP CER 470PF 1000V X7R 1206
XS1, XS2	DS1015-06-06R6SR	CONN HEADER VERT 6POS 2.54MM

The secondary winding of the planar power transformer, implemented on a multilayer printed circuit board to enhance isolation voltage, uses a 3C96 ferrite core size ER64/13/51 and is connected to a diode rectifier (synchronous rectification was deemed impractical due to low output current and limited PWM channels of the microcontroller). The transformer turns ratio NPri/NSec is approximately 0.2 (3/16) to achieve the target secondary-side voltage, accounting for dead-time at the minimum primary input voltage of 65 V. Maintaining the secondary voltage is critical for powering a downstream DC/AC converter connected to the common DC bus. The transformer parameters are given in *table 3*.

Table 3. Power transformer parameters

Parameter	Primary winding	Secondary winding
Number of turns	3	16
Inductance	117,5 uH	3,388 mH
Leakage inductance	0,2 uH	3,2 uH
Resistance	0,006 Ω	0,44 Ω
Design	Copper busbar	PCB

This DC/AC converter employs a full-bridge topology where each half-bridge generates positive and negative output voltage waves (measured between the midpoint of each half-bridge after the output LCL filter) [14, 15]. Thus, to produce an AC output with a peak voltage of 310 V (220 VRMS), considering voltage drops across the output filter and allowing margin for reactive loads, the minimum required secondary-side voltage is 340 V, which aligns with the calculated transformer ratio.

For measuring the current in the high-frequency power transformer, used in the current control loop of the system (which includes both current and voltage control loops) [16], and for protecting the converter against bridge shoot-through currents (short-circuit currents), a current sensor (current transformer) is installed in the positive busbar immediately before the power transistors, as shown in *figure 6*. The use of a current transformer is essential in high-frequency control loop designs for switched-mode power supplies due to its minimal measurement delay compared to other sensor types [17, 18].

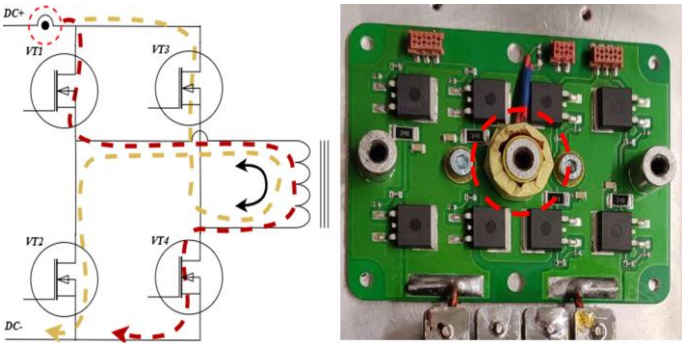

Figure 6. Current transformer location

The current transformer has a turns ratio of 1:200. Short-circuit protection is implemented using a comparator IC, where the voltage across the current transformer's burden resistor is compared to a set threshold. The comparator output is connected to a designated TZ pin of the microcontroller. When the current transformer signal exceeds the set threshold, the

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comparator output drives the TZ pin low, which disables the microcontroller's PWM peripheral module.

Measurements of the PSFB DC/DC converter's operation were conducted under constant active load conditions (using fixed resistors). The initial load value was 1.5 kW. The measured parameters matched the calculated values, and the converter operated stably. When the load was increased to the rated output power of 3 kW, the converter shut down due to triggering of the short-circuit protection (the comparator output driving the TZ pin low during operation). To analyze the ongoing processes, measurements of the voltage across the current transformer's burden resistor were taken with different time scales—1 µs and 2 µs. The measurements were taken on the current transformer resistor before the low-pass filter (RC circuit), the results are presented in *figure 7*.

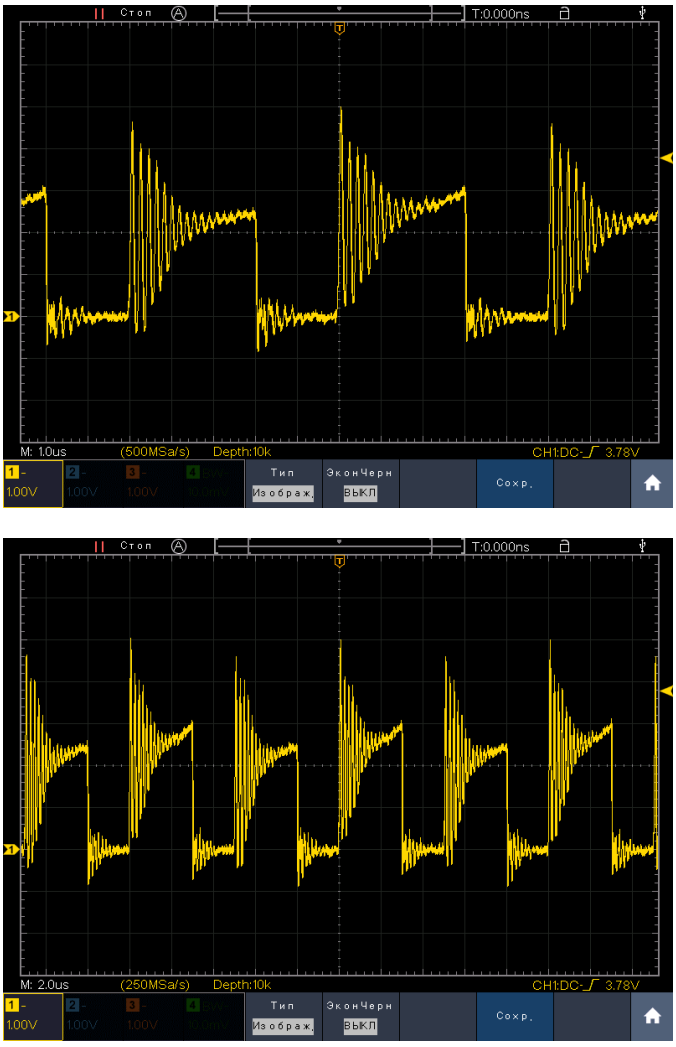

Figure 7. Oscillograms of the current of the primary winding of the transformer

Since the current transformer is installed in the DC+ busbar, the measured signal is unipolar and corresponds to the bidirectional current flowing through the primary winding of the power transformer.

According to the obtained oscillograms, a pronounced asymmetry in the current flow is observed. During the switching of transistors VT1-VT4, the current amplitude and waveform correspond to the calculated values and exhibit the correct shape with a slope angle characteristic of the charging inductance of the output LC filter installed after the diode rectifier. During the switching of transistors VT3-VT2, the peak current value exceeds the calculated value, and transformer saturation is observed, which is the cause of protection triggering. Moreover, the obtained waveforms are not typical for push-pull converters, as this type of switching power converter is designed to operate with symmetrical primary winding current.

Based on logical reasoning, the cause of the power transformer entering saturation (winding inductance approaches zero) in one of the operating cycles (switching of transistors VT3-VT2) could be an alteration in the operating duration of the power transistors. Since the developed software is implemented strictly according to the manufacturer's recommendations using the microcontroller's hardware ePWM module, only external circuit components could potentially influence changes in the PWM signal duration. For example, the 74HCT08D.653 AND logic gate IC installed for additional hardware protection of the power transistors.

For detailed analysis of the modifications introduced by the IC to the PWM signal duration, measurements were performed (*figure 8*). During these measurements, the minimum signal duration was set, and the microcontroller's hardware dead-time generation function was disabled.

Note about the oscilloscope: An AKTAKOM ADS-6144 oscilloscope with a 500 MHz bandwidth was used for circuit measurements. It provides a sampling rate of 5 GSa/s in single-channel mode and 2.5 GSa/s in dual-channel mode, the latter being necessary for accurately displaying signal propagation delays.

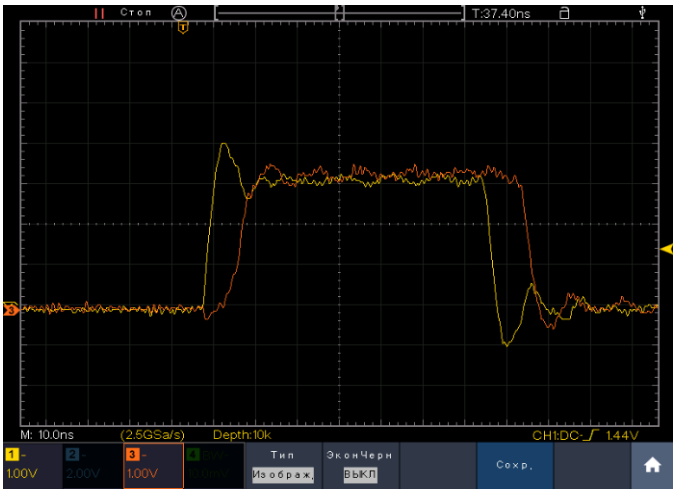

Figure 8. PWM signals before (yellow) and after (orange) the 74HCT08D.653 logic element

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The 74HCT08D.653 integrated circuit introduces a delay to the PWM signal of approximately 5–7 ns on the rising edge and 10–12.5 ns on the falling edge. These distortions in the PWM signal duration for the high-side transistors are the cause of transformer asymmetry due to different switching durations between transistors VT1-VT4 (EPWM1A EPWM2B) and VT2-VT3 (EPWM1B EPWM2A), leading to transformer saturation and, consequently, an increase in winding current [19, 20].

It should be noted that in classical PWM modulation (as opposed to phase-shifted modulation), where there are time intervals when all transistors are in the off state, the delay introduced into the PWM signal would affect the switching duration of both VT1-VT4 and VT2-VT3 transistors symmetrically [21]. Furthermore, when designing the bootstrap driver circuit shown in *figure 3*, a more correct solution would have been to generate the control signal for the lower transistors also through an AND logic gate IC to ensure symmetrical PWM signal delay for all transistors. However, due to the limited size of the control printed circuit board and single-sided component mounting, the two other channels of the 74HCT08D.653 IC were used to control optocouplers performing soft-start circuit switching and fan control functions.

4. SIMULATION OF THE PSFB CONVERTER PROTOTYPE

For a detailed analysis and to account for the influence of the delay introduced by the logic element, a model of the DC/DC converter was built in the MATLAB Simulink R2024a environment. *Figure 9* shows the converter model.

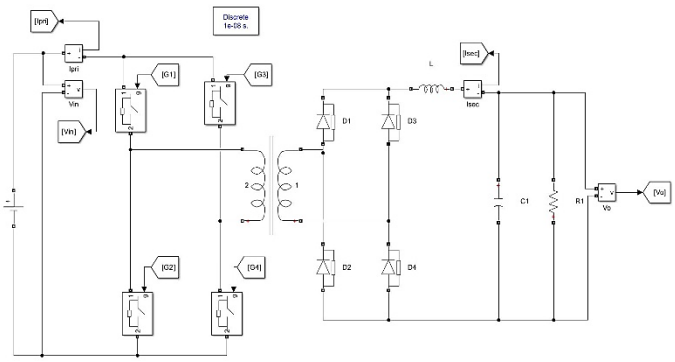
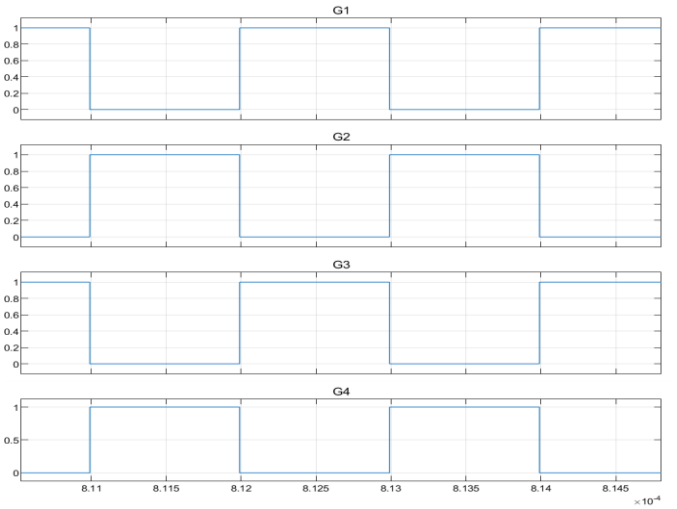
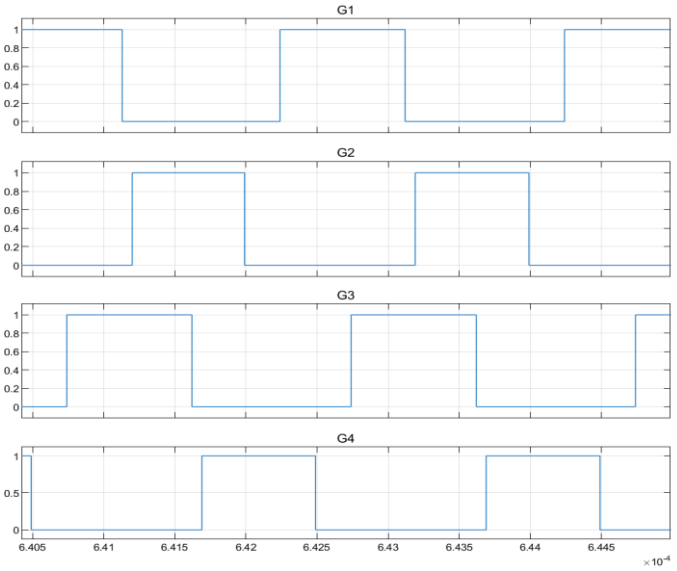


Figure 9. PSFB converter model in the MATLAB Simulink environment

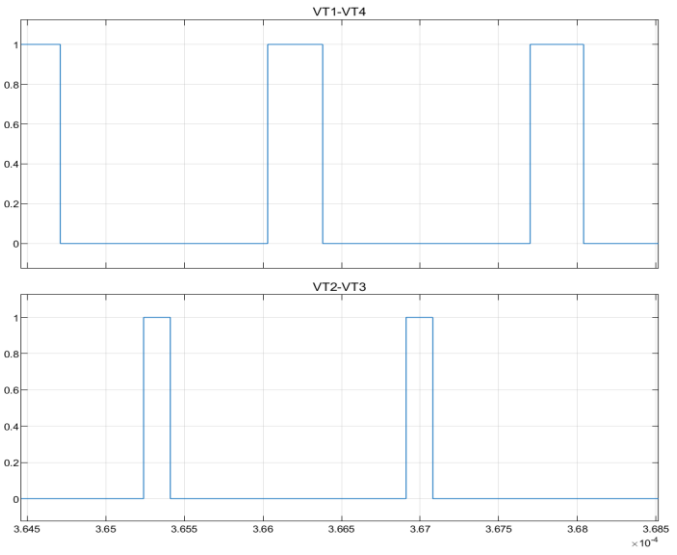
Next, a model for generating PWM signals with a dead-time of 200 ns was constructed, corresponding to the values set in the prototype. *Figure 10* shows oscillograms of PWM generation: *(a)* without phase shift and dead-time; *(b)* with a 50% phase shift and dead-time; *(c)* conduction phases of transistors VT1-VT4 and VT3-VT2 according to *figure 5*, with a 50% phase shift and a delay of 5 ns on the rising edge and 12.5 ns on the falling edge introduced by the logic element. For clarity, the PWM frequency was set to 500 kHz. Dead-time and the logic element delay were simulated using an On/Off Delay block.



(a)



(b)



(c)

Figure 10. Oscillograms of PWM signal generation and conduction phases

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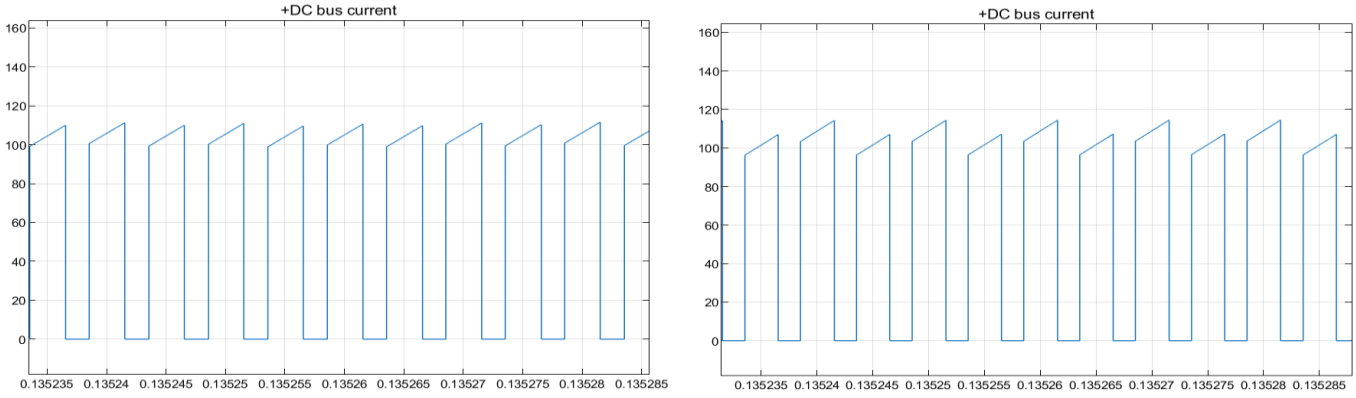
According to the obtained oscillograms, the most evident difference is the conduction time difference between VT1-VT4 and VT3-VT2, which amounts to 170 ns. *Figure 12* shows oscillograms of the +DC bus current from the developed converter model with an embedded phase-shift control system: (a) without delay; (b) with a signal delay corresponding to the 74HCT08D.653 IC.

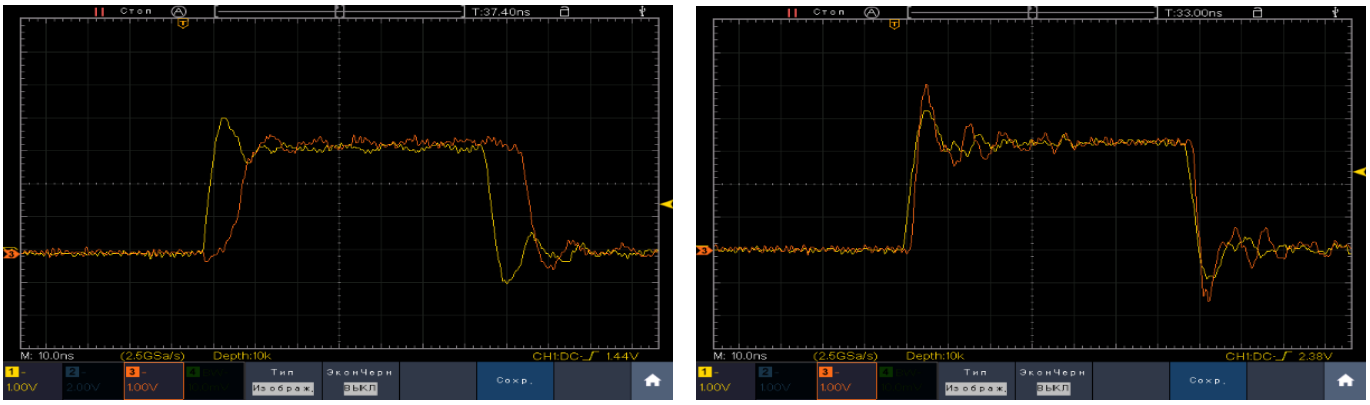


(a) *(b)*

Figure 11. Simulated oscillograms of the +DC bus current; (a) without signal delay; (b) with a signal delay corresponding to the 74HCT08D.653 IC

Thus, the mathematical simulation confirmed the direct influence of the 74HCT08D.653 control circuit element on the asymmetry of the currents flowing in the primary winding of the power transformer.

To avoid modifications to the control board circuitry while reducing the PWM signal delay introduced by the 74HCT08D.653 IC, yet preserving the hardware protection function against initial high-side transistor switching, an equivalent but faster IC from the same manufacturer was selected - the 74LVC08AD. Before conducting practical tests of the PSFB DC/DC prototype under nominal load, the 74LVC08AD IC underwent similar testing as the 74HCT08D.653 to measure its introduced PWM signal delays (*figure 12*).



(a) *(b)*

Figure 12. PWM signals before (yellow) and after (orange) the logic element; (left) — for the 74HCT08D.653 IC; (right)— for the 74LVC08AD IC

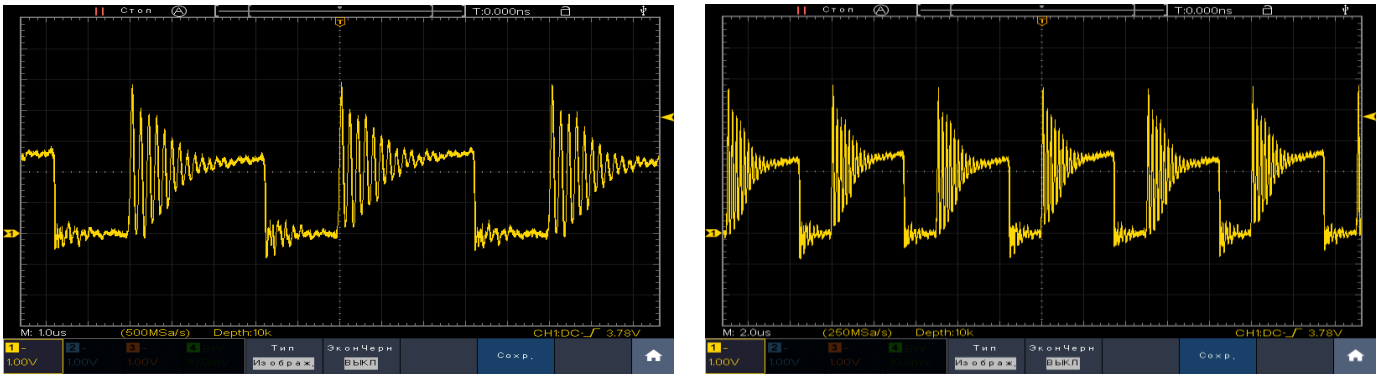


Figure 13. Oscillograms of the transformer primary winding current with 74LVC08AD

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Based on the obtained oscillograms, the developed prototype of the PSFB DC/DC converter operates stably, and the power transformer current is symmetrical. The measured values of the flowing current correspond to the calculated ones [22].

5. RESULTS

The design of modern high-frequency switched-mode DC/AC converters is a relevant task due to the growing trend toward green energy. Furthermore, the development and expansion of semiconductor components and integrated circuits enable the design of more cost-effective and efficient converters, as well as the implementation of alternative, previously unavailable solutions, such as a bootstrap driver circuit for safe control of SiC and MOSFET transistors rated for unipolar gate voltage.

In this study, the primary focus was on the design of the DC/DC section of the DC/AC converter, particularly the specifics of using a bootstrap driver circuit with additional hardware protection. It is important to note that the design solution examined is one of many possible approaches, and the final implementation largely depends on the criteria set for a specific device. In this case, the key requirement was the incorporation of additional protection.

The initially used AND logic gate IC, 74HCT08D.653, employed to introduce the ENABLE signal ("EN" *figure 3*), introduced a delay in the PWM control signal of approximately 5 ns on the rising edge and 12,5 ns on the falling edge, which was the cause of current asymmetry. Subsequent replacement of the 74HCT08D.653 IC with the 74LVC08AD practically eliminated the PWM signal delay, enabling symmetrical operation of the converter and maintaining the output voltage when connected to a nominal active load of 3 kW (*figure 14*).

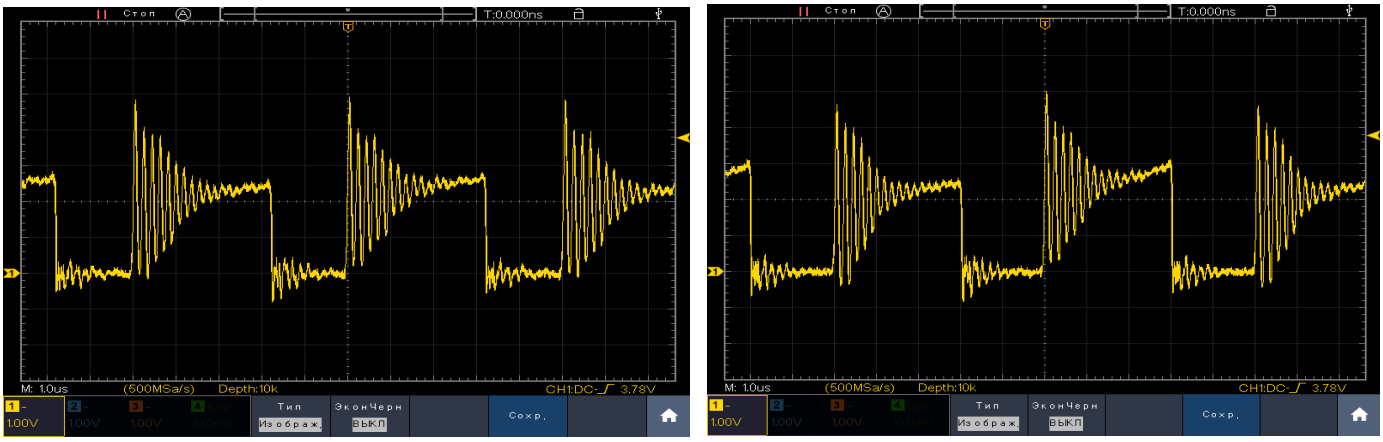

Figure 14. Oscillograms of the primary winding current of the transformer when using 74LVC08AD (left) and 74HCT08D.653 (right)

Further research is focused on the development of a complete DC/AC converter and analysis of the DC/AC section's impact on the developed DC/DC part. The main complexity lies in the sinusoidal nature of the power consumption, which also affects the amplitude of the high-frequency power transformer current and the operation of the control system as a whole.

The research findings can be useful and applied in educational processes and in the development of similar types of high-frequency converters.

Table 4. Comparative Result and Analysis

Parameter	74HCT08D.653	74LVC08AD
Control signal delay on rising edge	≈ 5 ns	≤ 2 ns
Falling edge control signal delay	≈ 12,5 ns	≤ 1 ns
Difference in primary winding current according to simulation results	≈ 10 A	≤ 1 A
Difference in primary winding current based on experimental measurements	≈ 20 A (due to saturation)	≤ 2 A

6. CONCLUSION

The conducted research enables a correct assessment of the influence of control signal delays for the upper transistors of the PSFB converter. The obtained results of mathematical modeling and experimental investigation confirm that a change in the control signal duration of less than 1% of the PWM period causes an asymmetry in the currents flowing through the primary winding and can lead to saturation of the power transformer. To ensure the symmetry of the currents flowing through the power transformer of the PSFB breadboard model, the 74HCT08D.653 logic IC was replaced with the faster 74LVC08AD. This minimized the signal delay (the signal delay is less than 2 ns for both rising and falling edges), and the asymmetry was reduced to less than 2 A.

Further research is focused on a more detailed study of the causes of asymmetric currents in the power transformer, the investigation of optimal operating modes, and the development of software solutions to reduce/account for the influence of delays on the control signals of logic elements.

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