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Symmetrical Sine-Carrier PWM-Based SVM for Performance Enhancement of Three-Phase Two-Level Wye Rectifier

Ong-ard Tubburee[1], and Kanyarat Ek-iam[2*]

[1]Department of Industrial Electrical Technology, Faculty of Industrial Technology, Valaya Alongkorn Rajabhat University under the Royal Patronage, Pathum Thani, Thailand; Email: ongart.tub@vru.ac.th
[2]Department of Industrial Electrical Technology, Faculty of Industrial Technology, Valaya Alongkorn Rajabhat University under the Royal Patronage, Pathum Thani, Thailand; Email: kanyarat@vru.ac.th

***Correspondence:** *kanyarat@vru.ac.th; Tel.: +668-3909-6155*

ABSTRACT- This paper proposes a symmetrical sine-carrier pulse width modulation (SSCPWM)-based space vector modulation (SVM) strategy for enhancing the performance of a three-phase two-level Wye rectifier. Unlike conventional triangular-carrier PWM (TCPWM) and inverted sine-carrier PWM (ISCPWM), the proposed method employs a symmetrical sinusoidal carrier waveform to reshape the pulse distribution while preserving the simplicity of comparator-based carrier PWM implementation. The modulation signals are generated from a current-sector-based SVM framework. These signals are then directly compared with the proposed carrier to generate the switching signals. Analytical expressions for the switching instants and duty ratios are derived to clarify the nonlinear carrier-crossing characteristics introduced by the sinusoidal carrier. The proposed method was evaluated under both open-loop and voltage-oriented control (VOC) operations using detailed MATLAB/Simulink simulations. The results demonstrated that the proposed SSCPWM achieved improved harmonic performance relative to TCPWM and ISCPWM schemes. The proposed method also reduced the DC-link voltage ripple. Comparable switching-loss characteristics were still preserved. Under VOC operation, the proposed method achieved a phase-current THD of 3.21%. This value corresponded to 16.0% and 16.8% reductions compared with TCPWM and ISCPWM, respectively. The DC-link voltage regulation performance remained comparable to that of the conventional methods. The proposed strategy exhibits improved transient current quality during load variations without increasing the switching frequency or modifying the conventional VOC structure. The results indicated that the proposed SSCPWM can provide a practically feasible solution for improving the power quality of a grid-connected two-level Wye rectifier.

Keywords: 3P-2L-Wye Rectifier, SSCPWM, Total Harmonic Distortion, DC-Link Voltage.

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1. INTRODUCTION

Three-phase pulse width modulation (PWM) rectifiers have been widely employed in modern power conversion systems due to their bidirectional current controllability, high power factor capability, and improved power quality characteristics. Depending on the converter structure and voltage level, three-phase PWM rectifiers are generally classified into two-level rectifiers (2LRs) and multilevel rectifiers (MLRs) [1, 2]. In applications requiring low DC-link voltage levels, 2LRs are very attractive because they eliminate neutral-point (NP) voltage control. Moreover, 2LRs employ only three controllable power switches (CPSs), whose number is only half of those used in conventional bridge rectifiers, to prevent a shoot-through fault and decrease the energy processing burden on CPSs [3]. Several configurations of 2LRs have been reported, including the three-phase two-level Wye (3P-2L Wye), 3P-2L Delta, and 3P-2L Bridge rectifiers. Among these configurations, the 3P-2L Wye rectifier has attracted considerable attention because of its reduced switch count, simple topology, elimination of neutral-point voltage balancing, and relatively low conduction loss compared with conventional bridge rectifiers [4–5]. Owing to these advantages, the 3P-2L Wye rectifier has been considered suitable for medium-power industrial converters, EV charging systems, and grid-connected power-conditioning applications. Despite these advantages, the 3P-2L Wye rectifier still suffers from relatively high input-current harmonic distortion because of its inherently two-level switching operation. Conventionally, current ripple and harmonic distortion can be reduced by increasing either the switching frequency or the input inductance. However, increasing the switching frequency significantly increases semiconductor switching losses and thermal stress. Meanwhile, larger passive inductors increase converter size, weight, cost, and stored magnetic energy. Therefore, improving current quality without increasing switching frequency remains an important research challenge for 2LR systems.

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To address this issue, various modulation and control strategies have been developed, such as carrier-based PWM (CBPWM), selective harmonic elimination PWM (SHEPWM), space vector modulation (SVM), and space vector pulse width modulation (SVPWM) [6–9]. The conventional CBPWM procedure is commonly used due to its simplicity. Still, it is restricted in terms of the utilization of DC-link voltage and presents clustered harmonic contents near the switching frequency. Alternative methods such as SHEPWM, random PWM (RPWM), and real-time harmonic control (RTHC) have been studied for enhanced spectral quality; however, these methods generally rely on offline nonlinear programming, random switching dynamics, and computationally intensive carrier generation strategies, which complicate the real-time feasibility [10]. Even though the SVM achieves higher voltage utilization and improved harmonic performance, sector identification and duty-cycle calculation are still required. This requirement increases the computational complexity and implementation burden increase, particularly for low-cost digital controllers. To overcome this limitation, carrier-based SVPWM (CB-SVPWM) is also developed, where SVM-generated modulating signals are directly compared with triangular carriers, resulting in a CBPWM pattern and thus combining the simplicity of the CBPWM approach and the high-performance advantage of SVM [3, 5]. Nevertheless, most existing carrier-based SVM strategies for rectifier systems still employ conventional triangular-carrier PWM (TCPWM). Although TCPWM offers linear switching characteristics and simple implementation, the constant carrier slope tends to produce clustered switching transitions. Such a switching characteristic produces concentrated harmonic sidebands near the switching-frequency region.

To improve harmonic performance, several carrier-shaping techniques have been investigated primarily for voltage-source inverter applications, and thus carrier-waveform shape substantially affects the performance of the fundamental component, the harmonic spectrum, and the output voltage [11]. Trapezoidal-carrier PWM has been reported to improve voltage utilization and reduce total harmonic distortion (THD) in multilevel inverters; however, it introduces increased mathematical complexity and nonuniform pulse distribution [12]. Sine–sine PWM techniques employing sinusoidal carriers and multiple sinusoidal references have also demonstrated improved harmonic spreading characteristics, but they require lookup tables and precalculated switching-angle information, thereby reducing implementation flexibility [13, 14]. Inverted sine-carrier PWM (ISCPWM) has been shown to improve spectral characteristics and voltage utilization under low modulation conditions [15-17]. However, the sharper carrier curvature near the carrier extrema often causes uneven pulse clustering in ISCPWM. This characteristic increases low-order harmonics at medium-to-high modulation indices and introduces additional implementation complexity associated with half-cycle carrier inversion.

Although carrier-waveform shaping has been extensively investigated for inverter applications, limited studies have analytically investigated the influence of smooth sinusoidal carrier redistribution on pulse generation, harmonic spectrum, DC-link voltage ripple, and semiconductor power losses in three-phase PWM rectifiers, particularly for the 3P-2L Wye topology. Furthermore, most existing studies focus primarily on steady-state voltage synthesis rather than the interaction between carrier-waveform characteristics and current-sector-based SVM operation under voltage-oriented control (VOC) [18, 19]. Consequently, a clear analytical comparison among TCPWM, ISCPWM, and smooth symmetrical sinusoidal carrier strategies for rectifier applications is still lacking. To address these limitations, this paper proposes a symmetrical sine-carrier PWM (SSCPWM)-based SVM strategy for the 3P-2L Wye rectifier. Unlike conventional TCPWM and ISCPWM methods, the proposed strategy employs a symmetrical sinusoidal carrier waveform to redistribute switching pulses more uniformly within each switching period while preserving the simplicity of comparator-based PWM implementation. A current-sector-based SVM framework is developed to derive closed-form analytical expressions for modulation signals, switching instants, and duty-cycle characteristics. Moreover, the effects of carrier-waveform shaping on harmonic performance, DC-link voltage ripple, switching losses, and rectifier efficiency are analytically investigated and compared with conventional TCPWM and ISCPWM schemes. The main contributions of this paper can be summarized as follows:

1. A SSCPWM strategy is proposed for the 3P-2L Wye rectifier to improve pulse distribution and current harmonic performance without increasing switching frequency.
2. A complete current-sector-based SVM analytical framework is developed for all twelve current sectors, including closed-form modulation signal derivations and sector-to-sector transformation relationships.
3. The influence of carrier-waveform shaping on switching instants, harmonic spectrum, DC-link voltage ripple, semiconductor power losses, and efficiency is analytically investigated.
4. Comprehensive simulation comparisons under both open-loop and VOC conditions are conducted against TCPWM and ISCPWM schemes, including FFT analysis, transient response evaluation, and semiconductor loss estimation.

The effectiveness of the proposed strategy was verified through detailed MATLAB/Simulink simulations under identical operating conditions.

2. TOPOLOGY AND OPERATION ANALYSIS OF 3P-2L-WYE RECTIFIER

2.1. Topology analysis

The circuit configuration of the 3P-2L Wye rectifier is illustrated in *figure 1*. The three-phase grid voltages are denoted as "e_{ig}" ($i \in \{a, b, c\}$) and are connected in series

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with input inductors (L_i), which limit current ripple and shape the grid currents. Each phase is interfaced with a diode-based front-end comprising upper and lower diodes, D_{iP} and D_{iN}, which provides unidirectional rectification to the DC bus. A boost-type conversion stage is realized using a modified phase-leg structure, where each leg consists of two simultaneously operating CPSs, S_{i1} and S_{i2}, together with their anti-parallel diodes. This configuration enables bidirectional current flow through the switches while maintaining unidirectional power transfer to the DC side. The three-phase legs are connected in a Wye configuration with a common neutral point, thereby forming a two-level rectifier topology with reduced switch count. On the DC side, a single DC-link capacitor (C) smooths the rectified voltage and provides energy buffering, while a resistive load (R_L) is connected across the DC link. Unlike multilevel rectifiers, the proposed topology does not require NP voltage balancing.

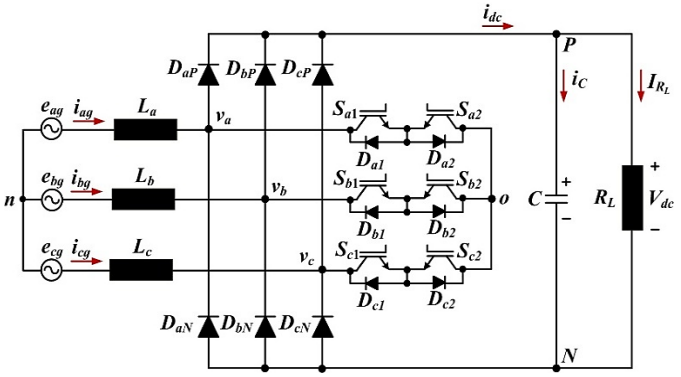

Figure 1. Topological structure of the 3P-2L Wye rectifier

2.2. Principle of Operation and Mathematical Model

The 3P-2L Wye rectifier operates by coordinating the switching of the CPSs (S_{i1} and S_{i2}), which control the input phase currents and the DC-link voltage at the same time. Each phase leg has two effective switching states corresponding to the connection of the phase terminal either to the positive DC bus (P) or to the negative DC bus (N). Consequently, the rectifier possesses eight possible switching states, consisting of six active states and two zero states, similar to a conventional two-level converter topology.

During the positive half-cycle of the grid voltage, the input current flows through the upper diode (D_{iP}), whereas during the negative half-cycle, the current commutates through the lower diode (D_{iN}). The anti-parallel diodes connected across the CPSs provide freewheeling paths under inductive loading conditions, thereby ensuring continuous current conduction. By appropriately selecting the switching states, sinusoidal input currents and regulated DC-link voltage can be achieved.

Assuming balanced three-phase grid voltages and identical input inductances, the AC-side dynamics of phase i can be described using Kirchhoff's voltage law (KVL) as

$$L_i \frac{di_{ig}}{dt} = e_{ig} - v_i \tag{1}$$

where L_i, e_{ig}, i_{ig}, and v_i denote the input inductance, grid phase voltage, grid phase current, and rectifier phase voltage of phase i, respectively. The rectifier phase voltage is determined by the switching function ($s_i \in \{0, 1\}$), which represents the connection state of the phase leg with respect to the DC bus, and can be expressed as

$$v_i = s_i V_{dc} \tag{2}$$

where V_{dc} denotes the DC-link voltage. On the DC side, the capacitor voltage dynamics are governed by Kirchhoff's current law (KCL), yielding

$$C \frac{dV_{dc}}{dt} = i_{dc} - \frac{V_{dc}}{R_L} \tag{3}$$

where C, i_{dc}, and R_L represent the DC-link capacitance, instantaneous output current, and load resistance, respectively. The instantaneous DC output current can be expressed as the weighted summation of the three-phase input currents according to their switching states:

$$i_{dc} = \sum_{i=a,b,c} s_i i_{ig} \tag{4}$$

Equations (1)-(4) establish the mathematical model of the proposed 3P-2L-Wye rectifier and clearly describe the coupling relationship between AC-side current control and DC-link voltage regulation. These equations form the analytical foundation for the modulation and control strategies.

3. CURRENT-SECTOR-BASED SVM COMMAND SIGNAL DESIGN

The primary objective of the current-sector-based SVM strategy is to generate appropriate modulation signals for the 3P-2L Wye rectifier such that the input currents accurately track the corresponding grid voltages with low harmonic distortion and near-unity power factor operation. In the conventional two-level SVM (2L-SVM) framework, the voltage vector plane is divided into six voltage sectors, denoted as VS_k (k = 1, 2, …, 6), each spanning 60°, as shown in *figure 2(a)*. However, for the 3P-2L Wye rectifier, the valid conduction paths depend not only on the location of the reference voltage vector but also on the instantaneous polarity of the input phase currents. Accordingly, each voltage sector is further subdivided into two regions according to the input phase current direction. The resulting sector division produces twelve equal regions with an angular width of 30°. These regions are referred to as current sectors (CS_n, n = 1, 2, …, 12), as illustrated in *figure 2(b)*. The introduction of current sectors enables accurate identification of conduction paths and appropriate selection of switching states for the 3P-2L Wye rectifier topology.

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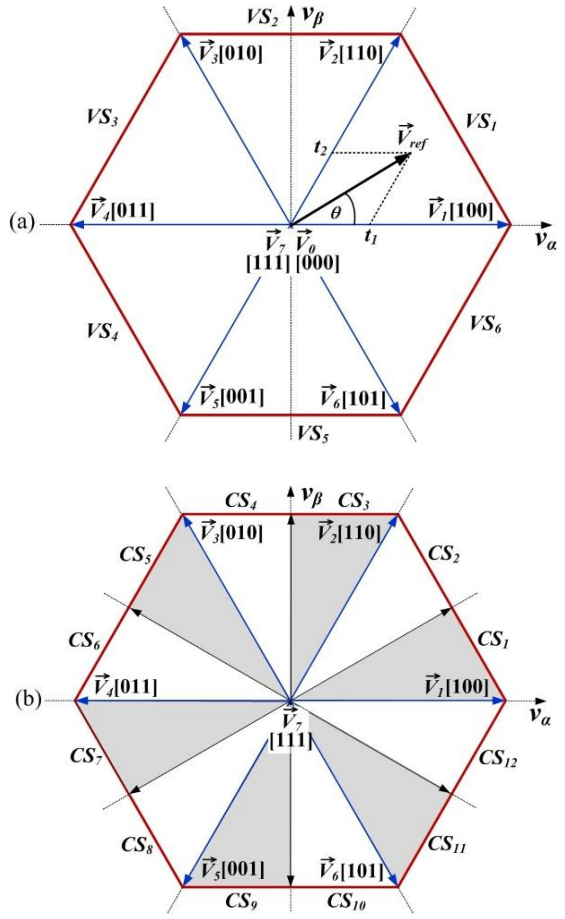

Figure 2. 2L-SVM diagram: (a) conventional 2L-SVM voltage sector division, and (b) 2L-SVM current sector division

Within each current sector, the reference voltage vector ($\vec{V}_{ref}$) is synthesized using two adjacent active vectors and one zero vector according to the conventional SVM principle. Taking CS_1 as an illustrative example, the $\vec{V}_{ref}$ is expressed as

$$\vec{V}_{ref} = \frac{t_1}{T_s}\vec{V}_1 + \frac{t_2}{T_s}\vec{V}_2 + \frac{t_7}{T_s}\vec{V}_7 \tag{5}$$

where T_s is the switching period, and t_1, t_2, and t_7 denote the dwell times of active vectors $\vec{V}_1$, $\vec{V}_2$, and the zero vector $\vec{V}_7$, respectively. Based on the conventional 2L-SVM relationship, the dwell times can be obtained as

$$\begin{cases} t_1 = T_s m_a sin\left(\frac{\pi}{3} - \theta\right) \\ t_2 = T_s m_a sin(\theta) \\ t_7 = T_s - t_1 - t_2 \end{cases} \tag{6}$$

where θ represents the angular position of the $\vec{V}_{ref}$ within the corresponding sector, and m_a is the modulation index defined as

$$m_a = \frac{\sqrt{3}|\vec{V}_{ref}|}{V_{dc}} \tag{7}$$

which directly reflects the DC-link voltage utilization capability of the modulation process. A symmetrical switching sequence is adopted to minimize switching transitions and ensure smooth commutation. Under this arrangement, only one phase leg changes its switching state during each commutation interval. When $\vec{V}_{ref}$ lies within CS_1, the symmetrical vector sequence $\vec{V}_1\vec{V}_2\vec{V}_7\vec{V}_2\vec{V}_1$ is adopted, as shown in *figure 3(a)*. Accordingly, the three-phase modulation signals are derived from the normalized accumulated dwell times as

$$\begin{cases} v_{ms,a} = \frac{t_1 + t_2 + t_7}{T_s} = 1 \\ v_{ms,b} = \frac{t_2 + t_7}{T_s} = 1 - m_a sin\left(\frac{\pi}{3} - \theta\right) \\ v_{ms,c} = \frac{t_7}{T_s} = 1 - m_a\left[sin\left(\frac{\pi}{3} - \theta\right) + sin\theta\right] \end{cases} \tag{8}$$

where $v_{ms,a}$, $v_{ms,b}$, and $v_{ms,c}$ denote the normalized modulation signals of phases a, b, and c, respectively.

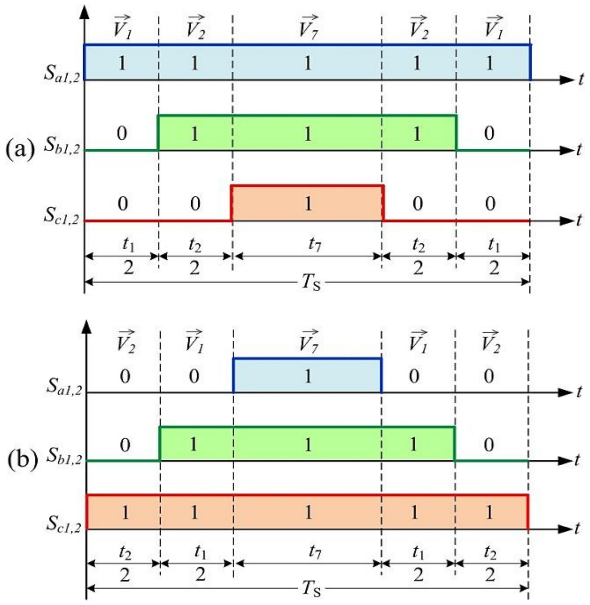

Figure 3. Symmetrical switching sequences for the 3P-2L Wye rectifier within one switching period: (a) gating signal arrangement in CS_1, and (b) gating signal arrangement in CS_2

In contrast, when the $\vec{V}_{ref}$ moves from CS_1 to CS_2, the adjacent active vectors remain unchanged; however, the switching states are inverted to satisfy the current polarity condition of the 3P-2L Wye rectifier, as illustrated in *fig.3(b)*. Accordingly, the modulation signals for CS_2 are expressed as

$$\begin{cases} v_{ms,a} = \frac{t_7}{T_s} = 1 - m_a\left[sin\left(\frac{\pi}{3} - \theta\right) + sin\theta\right] \\ v_{ms,b} = \frac{t_1 + t_7}{T_s} = 1 - m_a sin\theta \\ v_{ms,c} = \frac{t_1 + t_2 + t_7}{T_s} = 1 \end{cases} \tag{9}$$

After deriving the modulation equations for CS_1 and CS_2, the expressions for the remaining current sectors can be

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systematically obtained through sector-to-sector transformation. This transformation is based on two fundamental operations: phase-index rotation and switching-state inversion. The phase-index rotation follows the cyclic sequence $(a, b, c) \rightarrow (b, c, a) \rightarrow (c, a, b)$, which corresponds to the rotation of the reference voltage vector in the $\alpha\beta$-plane. Meanwhile, switching-state inversion is applied whenever the polarity of the corresponding input current changes between adjacent current sectors. For compact representation, let

$$A = m_a sin\left(\frac{\pi}{3} - \theta\right), \qquad B = m_a \sin\theta \tag{10}$$

Then, the modulation equations in CS_1 can be rewritten as

$$v_{ms,a} = 1, \quad v_{ms,b} = 1 - A, \quad v_{ms,c} = 1 - A - B$$

while the modulation equations in CS_2 become

$$v_{ms,a} = 1 - A - B, \quad v_{ms,b} = 1 - B, \quad v_{ms,c} = 1$$

The modulation equations for the remaining current sectors are subsequently generated by rotating the phase variables and adjusting the modulation polarity according to the current direction. Therefore, the complete set of modulation expressions for all twelve current sectors can be systematically derived without independently recalculating each sector. The resulting modulation equations are summarized in *table 1*.

Table 1. Modulating signal expressions for all current sectors

Current sectors	Three-phase modulation signal equations		
	$v_{ms,a}$	$v_{ms,b}$	$v_{ms,c}$
CS_1	1	$1 - m_a sin\left(\frac{\pi}{3} - \theta\right)$	$1 - m_a\left[sin\left(\frac{\pi}{3} - \theta\right) + sin\theta\right]$
CS_2	$1 - m_a\left[sin\left(\frac{\pi}{3} - \theta\right) + sin\theta\right]$	$1 - m_a sin\theta$	1
CS_3	$1 - m_a\left[sin\left(\frac{\pi}{3} - \theta\right) + sin\theta\right]$	$1 - m_a sin\theta$	1
CS_4	$1 + m_a sin\left(\frac{\pi}{3} - \theta\right)$	1	$1 - m_a sin\theta$
CS_5	$1 + m_a sin\left(\frac{\pi}{3} - \theta\right)$	1	$1 - m_a sin\theta$
CS_6	1	$1 + m_a sin\left(\frac{\pi}{3} - \theta\right)$	$1 + m_a sin\left(\frac{\pi}{3} + \theta\right)$
CS_7	1	$1 + m_a sin\left(\frac{\pi}{3} - \theta\right)$	$1 + m_a sin\left(\frac{\pi}{3} + \theta\right)$
CS_8	$1 + m_a sin\left(\frac{\pi}{3} + \theta\right)$	$1 + m_a sin\theta$	1
CS_9	$1 + m_a sin\left(\frac{\pi}{3} + \theta\right)$	$1 + m_a sin\theta$	1
CS_{10}	$1 + m_a sin\left(\theta - \frac{\pi}{3}\right)$	1	$1 + m_a sin\theta$
CS_{11}	$1 + m_a sin\left(\theta - \frac{\pi}{3}\right)$	1	$1 + m_a sin\theta$
CS_{12}	1	$1 - m_a sin\left(\frac{\pi}{3} - \theta\right)$	$1 - m_a\left[sin\left(\frac{\pi}{3} - \theta\right) + sin\theta\right]$

It should be noted that adjacent current-sector pairs exhibit identical mathematical forms, although their switching states and current polarities are different. Consequently, only six fundamental modulation patterns are required to cover all twelve current sectors, significantly simplifying the implementation complexity of the proposed SVM-based modulation strategy.

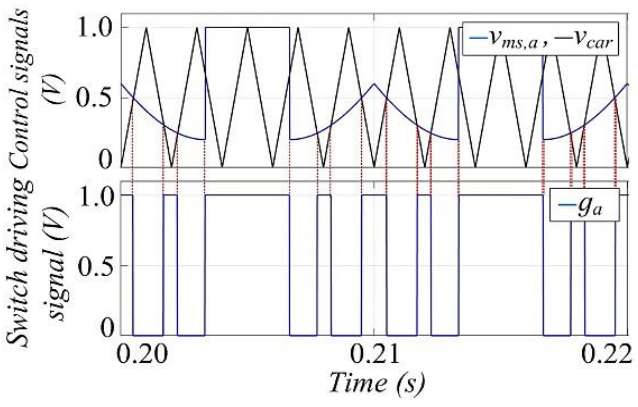
4. PROPOSED SSCPWM STRATEGY

In CBPWM schemes, the switching signals are generated by comparing a normalized modulating signal ($v_{ms,i}$), derived from the SVM dwell-time allocation, with a periodic carrier signal (v_{car}) operating at the switching frequency ($f_{sw} = 1/T_S$). For each phase leg, the binary switching function is defined as

$$g_i = \begin{cases} 1, & v_{ms,i} \geq v_{car} \\ 0, & v_{ms,i} < v_{car} \end{cases} \tag{11}$$

where g_i is subsequently mapped to the corresponding CPSs according to the current-sector-dependent switching states of the 3P-2L Wye rectifier. In conventional TCPWM, a symmetrical triangular carrier normalized within the range [0, 1] is commonly employed, as shown in *figure 4(a)*. Due to the constant carrier slope, the switching instants vary linearly with the modulation level, which generally produces concentrated harmonic sidebands around multiples of the switching frequency. Alternatively, the ISCPWM scheme shown in *fig. 4(b)* employs an inverted sine-wave carrier, which increases pulse concentration near the carrier extrema. Although this approach may improve voltage utilization at low modulation indices, it often produces uneven pulse spacing and increased harmonic distortion at moderate and high modulation regions.

(a)



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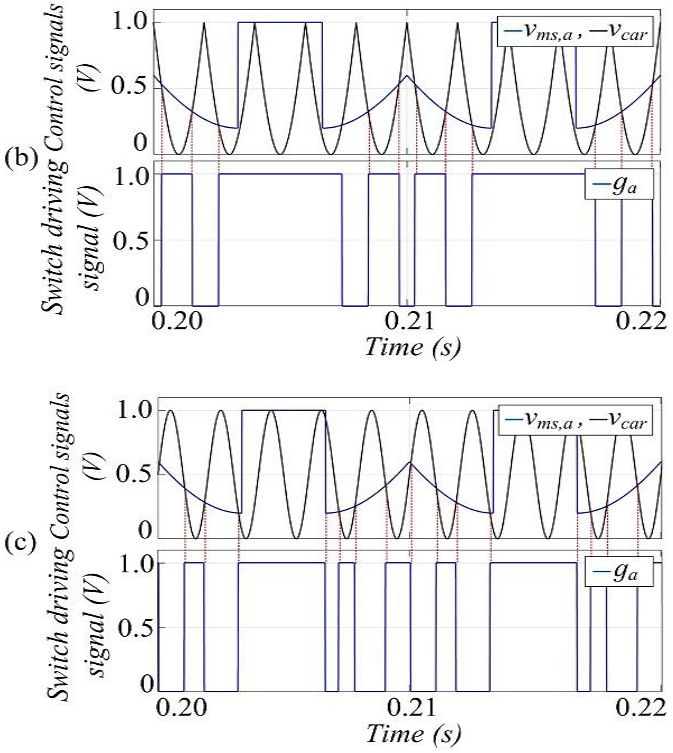

Figure 4. Switch driving signal generation for the 3P-2L-Wye rectifier: (a) conventional TCPWM scheme, (b) ISCPWM scheme, and (c) proposed SSCPWM strategy

To achieve a smoother pulse distribution while preserving the simplicity of comparator-based PWM, the proposed SSCPWM strategy, as shown in *figure 4(c)*, replaces the conventional triangular carrier and inverted sine-wave carrier with a symmetrical sinusoidal carrier normalized to the same range [0, 1], expressed as

$$v_{car} = \frac{1}{2}[1 + sin(2\pi f_{sw} t)], \quad 0 \le t < T_S \tag{12}$$

The carrier in *equation (12)* remains periodic and symmetrical within each switching cycle. Unlike TCPWM and ISCPWM, the proposed carrier reshapes the time relationship between the modulation signal and switching instants. Accordingly, the pulse positions are redistributed more uniformly throughout the switching period. Within one switching period, the switching instants for the *i*-phase are obtained from the carrier intersection condition.

$$v_{ms,i} = v_{car} \tag{13}$$

Assuming $v_{ms,i}$ remains quasi-constant during one sampling interval, which is a standard assumption in digital PWM, the carrier-crossing instants can be analytically obtained as

$$t_i^{\pm} = \frac{1}{2\pi f_{sw}}\left[(-1)^{\ell} sin^{-1}\left(2v_{ms\_i} - 1\right) + \pi\ell\right], \quad \ell \in \{0, 1\} \tag{14}$$

where the valid solutions $t_i^{(-)}$ and $t_i^{(+)}$ within $[0, T_S]$ define the turn-on and turn-off boundaries of the switching signal. Accordingly, the effective duty ratio of each phase leg can be expressed as

$$d_i = \frac{t_i^{(+)} - t_i^{(-)}}{T_S} \tag{15}$$

Unlike TCPWM, whose switching instants vary linearly with the modulation level, the proposed SSCPWM introduces a nonlinear yet smooth time mapping governed by the $sin^{-1}(\cdot)$ relationship. As a consequence, a more evenly distributed pulse pattern is obtained each switching period.

4.1. Harmonic Performance Analysis

The harmonic performance of carrier-based PWM schemes is strongly dependent on the pulse distribution generated within each switching period. In the TCPWM scheme, the linear carrier characteristic produces switching intervals proportional to the modulation signal.

$$d_i^{TCPWM} \propto v_{ms,i} \tag{16}$$

which tends to cluster switching transitions around specific carrier regions, thereby generating concentrated harmonic sidebands near multiples of the switching frequency. By contrast, the nonlinear carrier-crossing relationship of the proposed SSCPWM redistributes the switching instants more smoothly across the switching period. Therefore, abrupt pulse-width variations are reduced, resulting in a more evenly distributed harmonic spectrum and lower input current distortion. The input current THD is evaluated as

$$\%THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \times 100 \tag{17}$$

where I_1 is the fundamental current component and I_n denotes the n^{th} harmonic component. Owing to the smoother pulse distribution introduced by the sinusoidal carrier, the proposed SSCPWM effectively suppresses clustered switching harmonics relative to those produced by TCPWM and ISCPWM.

4.2. DC-Link Voltage Characteristics

The carrier waveform also affects the effective duty cycle distribution and consequently influences the DC-link voltage characteristics of the rectifier. The average DC-link voltage can be approximately expressed as

$$V_{dc} = \frac{3\sqrt{2}}{\pi}\left(\frac{V_{ph}}{1 - d_{eq}}\right) \tag{18}$$

where V_{ph} is the RMS phase voltage and d_{eq} denotes the equivalent duty ratio. In TCPWM and ISCPWM schemes, nonuniform pulse placement may lead to uneven instantaneous energy transfer, thereby increasing DC-link voltage fluctuation. The DC-link voltage ripple ratio is defined as

$$\%Ripple = \frac{V_{dc,max} - V_{dc,min}}{V_{dc,avg}} \times 100 \tag{19}$$

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where $V_{dc,max}$, $V_{dc,min}$, and $V_{dc,avg}$ represent the maximum, minimum, and average DC-link voltages, respectively. With the proposed SSCPWM, the smoother pulse distribution improves the continuity of instantaneous power transfer between the AC and DC sides. Consequently, capacitor charging and discharging become more uniform, reducing DC-link voltage ripple amplitude while slightly improving effective DC-link voltage utilization in the medium-to-high modulation region.

4.3. Switching Loss and Efficiency Analysis

Besides harmonic performance and DC-link voltage characteristics, the carrier waveform also influences the switching behavior and power loss distribution of the rectifier. In the proposed 3P-2L Wye rectifier, the total converter loss consists primarily of switching losses of the CPSs and conduction losses of both the CPSs and rectifier diodes [20]. The RMS phase current (I_{rms}), considering harmonic distortion, can be expressed as

$$I_{rms} = \frac{\hat{I}_1}{\sqrt{2}}\sqrt{1+THD^2} \tag{20}$$

where $\hat{I}_1$ is the fundamental peak current, and *THD* is the input current total harmonic distortion. The average switching current ($I_{sw,avg}$) is approximated by

$$I_{sw,avg} = \frac{2}{\pi}\hat{I}_1\sqrt{1+THD^2} \tag{21}$$

The switching energy (E_{sw}) is estimated using the datasheet-based scaling relationship

$$E_{sw} = E_{sw,rated}\left(\frac{V_{dc}}{V_{rated}}\right)\left(\frac{I_{sw,avg}}{I_{rated}}\right) \tag{22}$$

where $E_{sw,rated}$ denotes the switching energy specified in the device datasheet at the rated voltage V_{rated} and rated current I_{rated}. Accordingly, the total switching loss ($P_{sw,total}$) of the rectifier is obtained as

$$P_{sw,total} = 6f_{sw}E_{sw} \tag{23}$$

since the proposed rectifier employs six simultaneously operating CPSs. Furthermore, the conduction loss ($P_{cond,CPS}$) of the CPSs is calculated by

$$P_{cond,CPS} = 6I^2_{device,rms}R_{DS(on)} \tag{24}$$

where $I_{device,rms}$is the RMS current flowing through each CPS, and $R_{DS(on)}$is the on-state resistance of the selected switching device. Similarly, the conduction loss of the rectifier diodes ($P_{cond,D}$) is estimated as

$$P_{cond,D} = 6\left(V_{F0}I_{D,avg} + r_F I^2_{D,rms}\right) \tag{25}$$

where V_{F0} is the diode forward threshold voltage, r_F is the equivalent forward resistance, and $I_{D,avg}$ and $I_{D,rms}$ are the average and RMS diode currents, respectively. Consequently, the total converter loss ($P_{loss,total}$) can be expressed as

$$P_{loss,total} = P_{sw,total} + P_{cond,CPS} + P_{cond,D} \tag{26}$$

and the conversion efficiency (η) is determined by

$$\%\eta = \frac{P_{out}}{P_{out} + P_{loss,total}} \times 100 \tag{27}$$

where P_{out} is the output power of the rectifier. From *eq. (20)–(27)*, it can be observed that the switching and conduction losses are indirectly influenced by the harmonic content of the input current waveform. Since the proposed SSCPWM produces lower current THD compared with TCPWM and ISCPWM, the corresponding RMS and average switching currents are slightly reduced, resulting in lower conduction and switching losses. The smoother pulse distribution introduced by the symmetrical sine-wave carrier also mitigates abrupt switching transitions, thereby improving switching-energy distribution and reducing high-frequency switching stress.

5. Voltage-Oriented Control Design

The voltage-oriented control (VOC) method has been widely used in grid-connected converters since it is effective not only at suppressing DC-link voltage ripple and decreasing input current THD but also at achieving a unity power factor. In this research, to regulate the DC-link voltage and enhance grid-side power quality, a VOC scheme is employed for the 3P-2L Wye rectifier. The three-phase grid voltages and currents expressed in the stationary *abc* frame are transformed into a synchronous rotating *dq* reference frame aligned with the grid voltage vector. Under this alignment, the grid voltage is oriented along the *d*-axis, which simplifies the instantaneous power expressions. Accordingly, the active and reactive powers (P_g and Q_g) exchanged with the grid can be expressed as

$$\begin{cases} P_g = \frac{3}{2}v_{dg}i_{dg} \\ Q_g = -\frac{3}{2}v_{dg}i_{qg} \end{cases} \tag{28}$$

In this context, v_{dg} is the grid voltage component on the *d*-axis, while i_{dg} and i_{qg} are the corresponding current components on the *d*- and *q*-axes, respectively. From equation (28), it follows that the active power, and hence the DC-link voltage, is directly controlled by the *d*-axis current component, while the reactive power is governed by the *q*-axis current component. Therefore, DC-link voltage regulation is achieved by controlling i_{dg}. On the other hand, weighting i_{qg} = 0 leads to zero reactive power transfer and hence unity power factor operation.

6. SIMULATION RESULTS AND DISCUSSION

The performance of the proposed SSCPWM-based SVM for the 3P-2L Wye rectifier was verified through detailed time-domain simulations using MATLAB/Simulink. For a fair comparison, the proposed method was evaluated in comparison with conventional TCPWM- and ISCPWM-based

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SVM schemes under identical operating and control conditions. Both open-loop and VOC-based closed-loop operations were investigated to assess harmonic performance, DC-link voltage characteristics, dynamic response, and semiconductor power losses. The key system and device parameters used in the simulations and loss estimation are summarized in *table 2*.

Table 2. System and semiconductor parameters used in the simulations and loss estimation

Parameters	Symbol	Value
System parameters used in the simulations		
Output power	P_{out}	60 kW
DC-link voltage	V_{dc}	800 V
Grid voltage (RMS)	V_{ag}, V_{bg}, V_{cg}	230 V
Grid frequency	f_g	50 Hz
Switching frequency	f_{sw}	8 kHz
Input inductance	L_a, L_b, L_c	5 mH
DC-link capacitor	C	2200 µF
Semiconductor parameters for loss estimation		
CPS type	-	1200-V SiC MOSFET
MOSFET on-state resistance	$R_{DS(on)}$	45 mΩ
Reference switching energy	$E_{sw,rated}$	7.4 mJ
Rated voltage	V_{rated}	600 V
Rated current	I_{rated}	450 A
Diode forward voltage	V_{F0}	1.75 V
Diode forward resistance	r_F	2.5 mΩ

6.1. Open-loop comparison without VOC

The open-loop steady-state performance of the 3P-2L Wye rectifier using TCPWM, ISCPWM, and the proposed SSCPWM strategies is summarized in Table 3 over a wide modulation range ($0.1 \leq m_a \leq 1.0$). The results demonstrated that the proposed SSCPWM consistently achieved lower input-current THD as compared with both TCPWM and ISCPWM over most practical operating conditions ($0.3 \leq m_a \leq 0.9$). This tendency became more noticeable in the medium-to-high modulation region ($0.5 \leq m_a \leq 0.9$), where the THD decreased to approximately 19.61%–24.08%. The improvement mainly originates from the smoother pulse redistribution of the symmetrical sinusoidal carrier. As a result, switching harmonics became less concentrated. The switching intervals were also more evenly distributed. The ISCPWM scheme showed the highest THD, especially at high modulation indices. The higher distortion mainly originates from the nonuniform pulse concentration near the carrier extrema, which increases harmonic clustering and deteriorates the current waveform quality.

The displacement power factor (DPF) of all methods remained close to unity owing to the inherent current-tracking capability of the SVM framework. However, because of its lower harmonic distortion, the proposed SSCPWM also achieved the highest overall power factor (PF) across most modulation conditions. In terms of voltage characteristics, TCPWM and SSCPWM exhibited comparable DC-link voltage levels throughout the modulation range, whereas ISCPWM generally produced slightly higher DC-link voltages at low modulation indices due to pulse concentration around the carrier peaks. Nevertheless, this increased voltage utilization was accompanied by larger THD and higher DC-link ripple ratios. At m_a = 0.1, both TCPWM and ISCPWM became inoperable because the modulating signals remained close to unity for extended intervals. As a result, the switching function remained at logic state "1" for prolonged durations. This effect was more pronounced for the triangular and inverted-sine carriers due to their sharp carrier slopes near the peak regions. These steep carrier characteristics delayed the carrier-crossing instants and significantly reduced effective switching transitions. Under this condition, the CPSs tended to remain in a quasi-permanent ON state, thereby preventing proper pulse modulation, DC-link voltage regulation, and input-current shaping. In contrast, the proposed SSCPWM remained operable under this condition because its smoother nonlinear carrier-crossing characteristic preserved effective pulse generation even at extremely low modulation indices.

Table 3. Steady-state performance comparison of carrier-based SVM schemes for the 3P-2L Wye rectifier

Modulation index	Performance indices	TC-PWM	ISC-PWM	SSC-PWM
0.1	Input current THD (%)	Not Operable	Not Operable	33.48
	DPF (%)			98.46
	PF (%)			93.36
	Average DC-link voltage (V)			2,674
	DC-link voltage ripple ratio (%)			0.22
0.2	Input current THD (%)	30.18	48.76	31.53
	DPF (%)	97.92	94.81	99.46
	PF (%)	93.75	85.22	94.86
	Average DC-link voltage (V)	3,281	4,250	1,944
	DC-link voltage ripple ratio (%)	0.22	0.24	0.30
0.3	Input current THD (%)	28.53	46.21	27.32
	DPF (%)	99.13	97.59	99.56
	pf (%)	95.33	88.59	96.04
	Average DC-	1,785	2,601	1,476

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	link voltage (V)			
	DC-link voltage ripple ratio (%)	0.39	0.39	0.40
0.4	Input current THD (%)	27.79	42.53	24.87
	DPF (%)	99.36	98.72	99.72
	PF (%)	95.73	90.84	96.77
	Average DC-link voltage (V)	1,381	2,009	1,243
	DC-link voltage ripple ratio (%)	0.46	0.50	0.47
0.5	Input current THD (%)	27.05	40.24	24.08
	DPF (%)	99.43	99.53	99.92
	PF (%)	95.98	92.33	97.14
	Average DC-link voltage (V)	1,135	1,633	1,116
	DC-link voltage ripple ratio (%)	0.54	0.60	0.52
0.6	Input current THD (%)	26.33	38.97	22.25
	DPF (%)	99.80	99.56	99.92
	PF (%)	96.51	92.76	97.53
	Average DC-link voltage (V)	969	1,358	976
	DC-link voltage ripple ratio (%)	0.63	0.69	0.59
0.7	Input current THD (%)	26.11	35.25	21.01
	DPF (%)	99.76	99.56	99.89
	PF (%)	96.53	93.89	97.75
	Average DC-link voltage (V)	801	1,143	875
	DC-link voltage ripple ratio (%)	0.74	0.80	0.66
0.8	Input current THD (%)	25.56	33.71	19.61
	DPF (%)	99.72	99.56	99.87
	PF (%)	96.61	94.34	98.01
	Average DC-link voltage (V)	698	958	783
	DC-link voltage ripple ratio (%)	0.85	0.97	0.74
0.9	Input current THD (%)	24.84	35.00	20.13
	DPF (%)	99.67	99.40	99.84
	PF (%)	96.63	93.82	97.88
	Average DC-link voltage (V)	627	834	703
	DC-link voltage ripple ratio (%)	0.93	1.12	0.84
1.0	Input current THD (%)	21.78	42.30	27.68
	DPF (%)	99.59	99.13	99.53
	PF (%)	97.30	91.30	95.52
	Average DC-link voltage (V)	568	683	611
	DC-link voltage ripple ratio (%)	1.01	1.42	1.06

6.2. VOC Steady-State Performance

Figures 5–7 compared the steady-state performance of the 3P-2L Wye rectifier using TCPWM-, ISCPWM-, and proposed SSCPWM-based SVM schemes under the VOC framework. As shown in *figures 5(a)–7(a)*, all methods successfully regulated the DC-link voltage around the nominal value of 800 V. The conventional TCPWM produces an average DC-link voltage of 797 V, corresponding to a voltage regulation of 0.38%, whereas both ISCPWM and the proposed SSCPWM achieve an average voltage of 801 V with improved regulation of 0.13%. The proposed SSCPWM also provided the lowest DC-link voltage ripple of 6.23 V, compared with 6.96 V for TCPWM and 7.83 V for ISCPWM. The reduced ripple characteristic can be linked to the smoother switching-pulse distribution generated by the symmetrical sinusoidal carrier. The more uniform pulse arrangement improves instantaneous power-transfer continuity and contributes to better DC-side power quality. The voltage waveforms in *figures 5(b)–7(b)* confirmed that all schemes preserve the conventional two-level switching structure of the 3P-2L Wye rectifier, where the pole voltage consists of three discrete levels (±Vdc and 0). Hence, the observed performance improvement originates solely from carrier-waveform modification without altering the converter topology or switching sequence.

The superiority of the proposed SSCPWM became more evident in the current waveforms and FFT spectra shown in *figures 5(d)–7(d)*. Under TCPWM operation, the measured phase-current THD was 3.82%, with dominant harmonic sidebands concentrated around the switching-frequency region. For ISCPWM, the THD slightly increased to 3.86% due to the sharper carrier curvature, which produced less uniform switching intervals and additional low-order harmonic components. As compared with TCPWM and ISCPWM, the proposed SSCPWM achieved the lowest THD of 3.21%. A noticeable reduction in the dominant switching-frequency sidebands can also be observed from the FFT spectrum. The harmonic components were also distributed more evenly over the frequency range. This behavior was mainly caused by the smoother nonlinear time mapping introduced by the symmetrical sinusoidal carrier, which redistributed the switching instants more gradually within each switching cycle. Overall, the proposed SSCPWM achieved 16.0% and 16.8% relative THD reduction relative to TCPWM and ISCPWM, respectively. These improvements were obtained without increasing the switching frequency or modifying the VOC

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structure. These results confirm that the proposed method effectively improved the current waveform quality. The DC-link voltage regulation capability and implementation simplicity were still preserved.

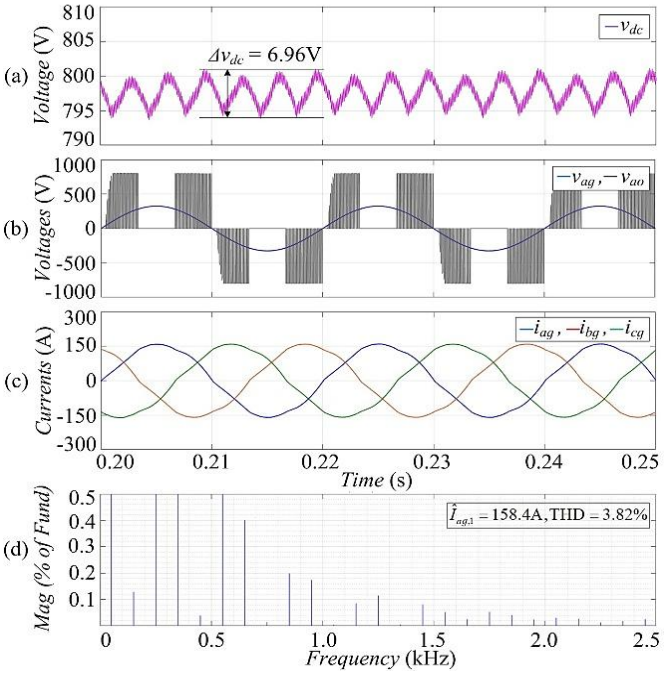

Figure 5. Steady-state performance of the 3P-2L Wye rectifier using conventional TCPWM-based SVM with VOC scheme: (a) DC-link voltage, (b) a-phase and pole voltages, (c) three-phase currents, and (d) phase current THD

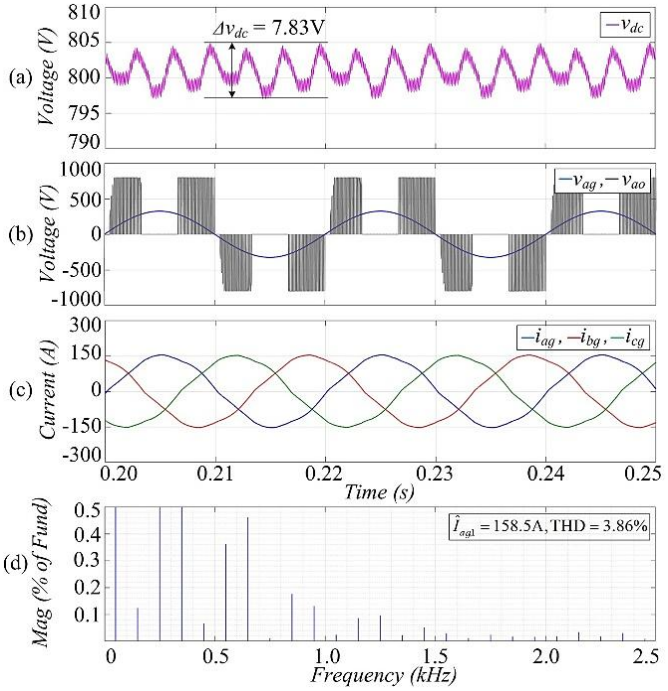

Figure 6. Steady-state performance of the 3P-2L Wye rectifier using the ISCPWM-based SVM with VOC scheme: (a) DC-link voltage, (b) a-phase and pole voltages, (c) three-phase currents, and (d) phase current THD

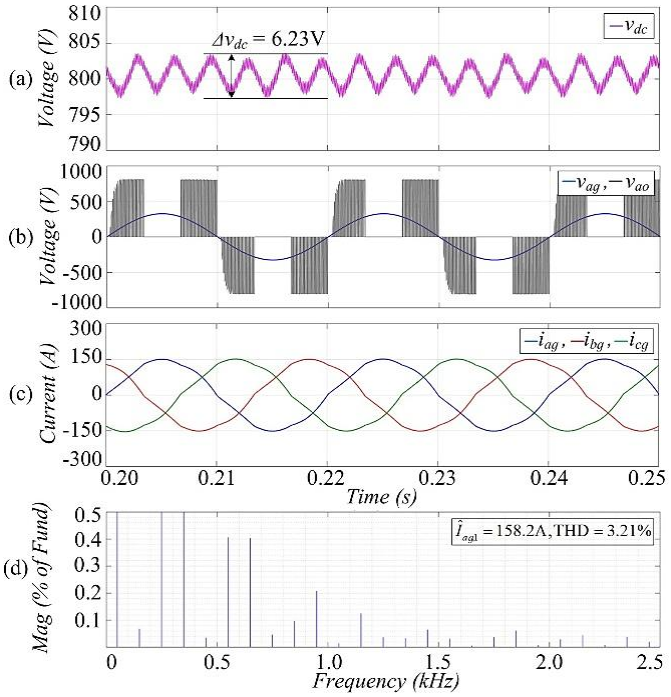

Figure 7. Steady-state performance of the 3P-2L Wye rectifier using the proposed SSCPWM-based SVM with VOC scheme: (a) DC-link voltage, (b) a-phase and pole voltages, (c) three-phase currents, and (d) phase current THD

As summarized in *table 4*, the proposed SSCPWM achieves the lowest estimated total semiconductor loss among the investigated carrier-based SVM schemes. Although the switching-loss differences among the three methods are relatively small due to the identical switching frequency, the reduced THD obtained by the proposed method slightly decreases both the RMS conduction current and average switching current. Consequently, the proposed SSCPWM produces the lowest conduction losses in both the CPSs and rectifier diodes, resulting in a total estimated semiconductor loss of 1480.21 W and an efficiency of 97.592%. By comparison, TCPWM and ISCPWM exhibit slightly higher total losses of 1483.20 W and 1484.54 W, respectively.

Table 4. Estimated switching loss, conduction loss, and efficiency comparison of carrier-based SVM schemes for the 3P-2L Wye rectifier

Method	THD (%)	P_{sw} (W)	$P_{cond,CPS}$ (W)	$P_{cond,D}$ (W)	Total loss (W)	Efficiency (%)
TCPWM	3.82	473.62	177.15	832.43	1483.20	97.588
ISCPWM	3.86	473.93	177.38	833.23	1484.54	97.586
SSCPWM	3.21	472.92	176.62	830.66	1480.21	97.592

6.3. Dynamic response

Figures 8–10 compared the dynamic responses of the 3P-2L Wye rectifier using the TCPWM, ISCPWM, and proposed SSCPWM strategies under identical transient operating conditions. In this test, the load power was reduced to 50% of the rated value at $t = 3.5$s and restored to the rated load at $t =$

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3.6s. The corresponding reduction and recovery of the load current can be clearly observed in *figures 8(a), 9(a)*, and *10(a)*. The DC-link voltage responses shown in *figures 8(b), 9(b),* and *10(b)* indicate that all modulation schemes exhibited a similar transient behavior during the load variation. In each case, the average DC-link voltage experienced a temporary step increase of approximately 3 V immediately after the load reduction due to the instantaneous mismatch between the input and output power. Nevertheless, the VOC framework rapidly restored the DC-link voltage to its reference value, demonstrating stable closed-loop regulation for all carrier-based PWM methods. The results also showed that the proposed SSCPWM remained fully compatible with the conventional VOC structure. No noticeable degradation in voltage-control performance or dynamic response characteristics was observed during the transient operation.

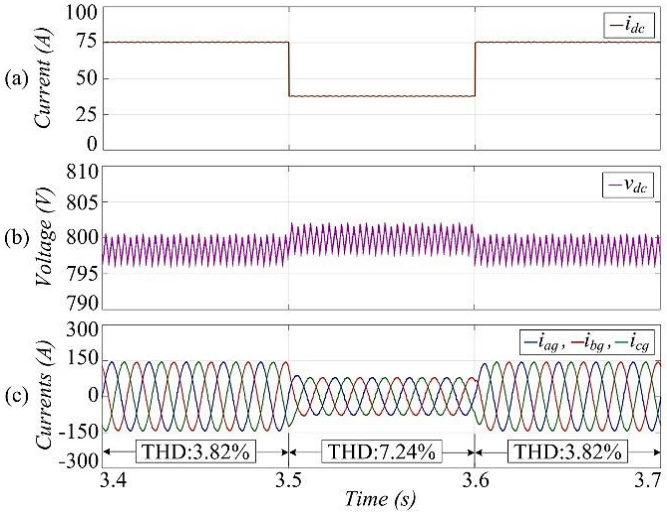

Figure 8. Dynamic performance of the 3P-2L Wye rectifier using conventional TCPWM-based SVM with VOC scheme: (a) load current, (b) DC-link voltage, and (c) three-phase currents

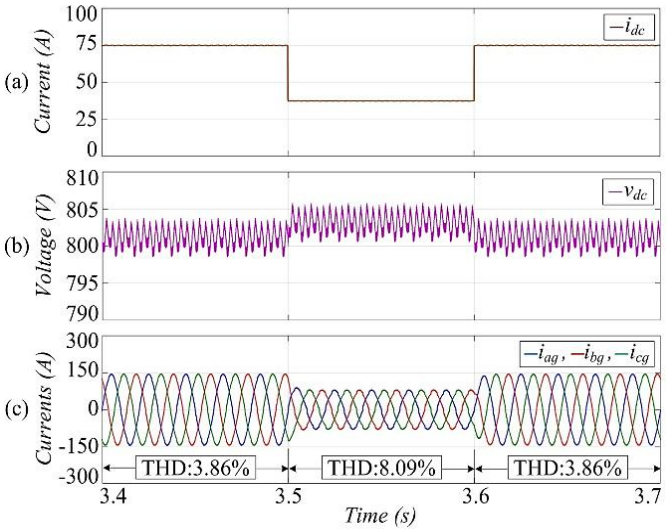

Figure 9. Dynamic performance of the 3P-2L Wye rectifier using the ISCPWM-based SVM with VOC scheme: (a) load current, (b) DC-link voltage, and (c) three-phase currents

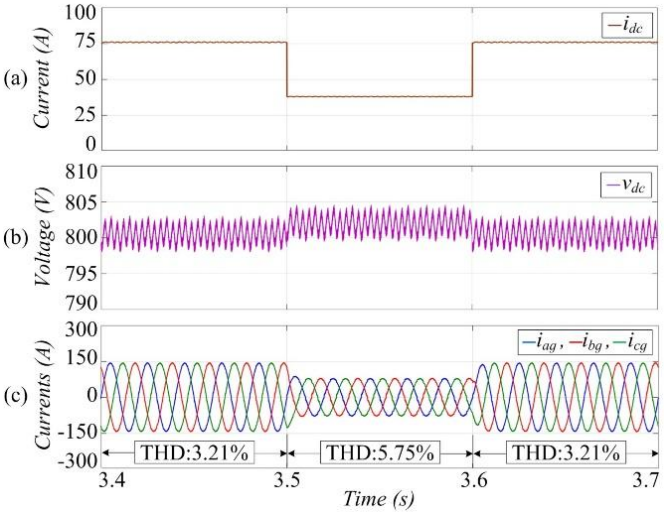

Figure 10. Dynamic performance of the 3P-2L Wye rectifier using the proposed SSCPWM-based SVM with VOC scheme: (a) load current, (b) DC-link voltage, and (c) three-phase currents

Despite the similar DC-link voltage responses, noticeable differences can be observed in the input current waveforms and harmonic characteristics during the transient interval. As illustrated in *figures 8(c)–10(c)*, the proposed SSCPWM maintained balanced and sinusoidal three-phase input currents throughout both the rated-load and reduced-load conditions. The corresponding FFT results also demonstrated that the proposed method consistently achieved lower phase-current THD in comparison with the TCPWM and ISCPWM schemes under both steady-state and transient operating conditions. Overall, the proposed strategy improved both steady-state and transient current quality. The results further indicated improved dynamic stability under varying load conditions, making the method suitable for grid-connected rectifier applications.

7. PRACTICAL IMPLEMENTATION FEASIBILITY AND LIMITATIONS

The proposed SSCPWM preserves the comparator-based simplicity of conventional CBPWM while improving harmonic performance. Compared with TCPWM, the proposed method only replaces the triangular carrier with a sinusoidal carrier, resulting in only a slight increase in computational burden. In contrast to ISCPWM, the proposed SSCPWM avoids half-cycle carrier inversion and associated polarity-transition logic, thereby simplifying real-time implementation. From a practical implementation viewpoint, the proposed strategy does not rely on additional sensors, predictive algorithms, or online dwell-time recalculation. The method can be directly integrated into conventional DSP- or FPGA-based PWM platforms using standard sinusoidal carrier generation and comparator operations, while retaining the same current-sector switching table as conventional SVPWM.

The improvement in current quality is achieved solely through carrier-waveform reshaping without increasing the switching frequency or modifying the VOC structure. As a result, the

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proposed method maintains comparable switching loss and efficiency characteristics. At the same time, lower current THD and DC-link voltage ripple are obtained. At this stage, the proposed strategy has been validated through analytical and simulation-based studies to isolate the influence of carrier-waveform shaping from hardware-dependent nonidealities, such as parasitic effects, sensor noise, and gate-driver delays. Although hardware validation is not included, the proposed SSCPWM requires no additional power devices or auxiliary circuits beyond conventional SVPWM structures. This characteristic indicates strong feasibility for practical real-time implementation in grid-connected rectifier systems.

8. CONCLUSIONS

This paper presented a symmetrical sine-carrier PWM (SSCPWM)-based SVM strategy for the three-phase two-level Wye (3P-2L Wye) rectifier. Instead of using the conventional triangular carrier, the proposed method employs a symmetrical sinusoidal carrier to redistribute the switching pulses more smoothly. The carrier-crossing behavior is therefore modified while the simplicity of carrier-based PWM implementation is still preserved. A current-sector-based SVM framework and analytical derivation of switching instants and duty ratios were developed to describe the operating principle of the proposed modulation strategy. Simulation results under both open-loop and VOC conditions demonstrated that the proposed SSCPWM achieves superior harmonic performance relative to TCPWM and ISCPWM schemes. Under VOC operation, the proposed method reduced the phase-current THD to 3.21%. This value corresponded to 16% lower distortion than the conventional methods. Comparable DC-link voltage regulation and switching loss characteristics were also maintained. In addition, the proposed method exhibited lower DC-link voltage ripple and improved transient current quality during load variations. The estimated switching loss, conduction loss, and efficiency analysis further confirmed that the proposed carrier modification improved waveform quality without increasing switching frequency or significantly affecting converter efficiency.

The proposed SSCPWM also maintains the implementation simplicity of conventional carrier-based PWM because it does not require additional sensors, predictive algorithms, or complex online optimization routines. Overall, the proposed method provides a practical approach for improving the power quality of grid-connected 3P-2L Wye rectifiers. The implementation complexity remains comparable to that of conventional carrier-based PWM schemes. Future work will focus on experimental validation using a real-time DSP/FPGA-based hardware prototype under practical operating conditions.

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