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International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 14, Issue 2 | Pages 553-561 | e-ISSN: 2347-470X

# A Novel DC-DC Buck Converter for Portable Applications

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**ABSTRACT-** This paper presents a simple pulse-generator-based DC–DC buck converter capable of adaptive ripple reduction and automatic CCM/DCM mode transition over a wide load-current range. The proposed converter consists of a pulse generator, a buffer and dead-time circuit, and complementary PMOS/NMOS power switches. Unlike conventional hysteretic buck converters, the proposed pulse generator dynamically adjusts the switching operation according to the load condition by monitoring the PMOS conduction current. Consequently, reverse inductor current is suppressed under light-load conditions, enabling automatic transition between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) without requiring additional mode-control circuitry. Simulation results based on a 0.18-µm CMOS process demonstrate that the proposed converter operates over a load-current range from 0 mA to 500 mA with a switching frequency ranging from 310 kHz to 3.50 MHz. At a load current of 500 mA, the converter achieves an output-voltage ripple of 372.4 µVp-p and an output-current ripple of 4.95 mAp-p. In addition, transient recovery times of 6.9 µs and 4.5 µs are achieved for load-current transitions from 0 mA to 500 mA and from 500 mA to 0 mA, respectively. The proposed converter achieves a peak power efficiency of 85% while providing low ripple characteristics, automatic operating-mode transition, reverse-current suppression, and a simple control architecture.

**Keywords:** DC-DC Buck Converter, Voltage-Driven Method, Voltage ripple, Current Ripple.

**ARTICLE INFORMATION**

**Author(s)**: Chae-Hyoung Choi, Seung-Hyun Jeong, and Sung-Sik Park;
**Received**: 07/03/26; **Accepted**: 13/06/26; **Published**: 30/06/26;
**E- ISSN**: 2347-470X;
**Paper Id**: IJEER 0703B05;
**Citation**: 10.37391/ijeer.140230
**Webpage-link**:
https://ijeer.forexjournal.co.in/archive/volume-14/ijeer-140230.html



## 1. INTRODUCTION

DC–DC buck converters are widely employed in portable electronic devices, battery-powered systems, and power-management integrated circuits (PMICs) owing to their high power-conversion capability and compatibility with low-voltage mixed-signal systems. As the demand for low-power, high-efficiency, and high-performance portable applications continues to increase, considerable research efforts have been devoted to improving converter characteristics such as power-conversion efficiency, output-voltage ripple, transient response, load-current range, and operational stability [1]–[20]. Among various control schemes, hysteretic DC–DC buck converters have attracted significant attention because of their simple architecture, fast transient response, and inherent stability. However, conventional hysteretic converters generally exhibit relatively large output-voltage and inductor-current ripples, particularly under light-load conditions, resulting in degraded power-conversion efficiency. To improve the performance of hysteretic converters, adaptive window control (AWC) techniques have been introduced to dynamically adjust the hysteresis window according to load conditions [22]. Although the AWC approach improves converter performance over a wide load range, it requires additional circuitry for hysteresis-window generation and mode-transition control, thereby increasing implementation complexity.

Recent DC–DC buck and buck–boost converters have adopted advanced control techniques such as load-current prediction [16], V-square control [17], tri-mode operation [18], digital dual-mode control [19], enhanced hysteresis control [20], and three-mode selection control [21]. These approaches achieve improved power-conversion efficiency, fast transient response, and seamless mode transition over a wide load-current range. Nevertheless, most of these techniques rely on additional current-sensing circuits, adaptive control blocks, predictive algorithms, digital controllers, or dedicated mode-selection logic, leading to increased circuit complexity, silicon area, and power consumption. Furthermore, advanced converter-control methodologies based on feedback-control and state-space analysis have been investigated to improve regulation accuracy and stability [23]. Although these approaches provide enhanced operating characteristics, their implementation typically requires more sophisticated control mechanisms and additional hardware resources.

Therefore, a DC–DC buck converter capable of achieving low ripple, fast transient response, and automatic conduction-mode transition while maintaining a simple circuit architecture remains highly desirable for portable power-management applications.

To address these challenges, this paper proposes a voltage-driven DC–DC buck converter employing a simple pulse-generator architecture. The proposed pulse generator dynamically adjusts the switching pulse width according to

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Research Article | Volume 14, Issue 2 | Pages 553-561 | e-ISSN: 2347-470X

load-current-dependent output-voltage variations, enabling automatic transition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Unlike conventional load-current prediction, tri-mode, digital dual-mode, and three-mode selection approaches, the proposed technique does not require explicit inductor-current sensing, adaptive hysteresis-window control, predictive computation, or dedicated mode-selection logic. In addition, reverse-current conduction under light-load conditions is effectively suppressed, while both output-voltage ripple and inductor-current ripple are significantly reduced.

The main contributions of this work are summarized as follows.

1. A simple voltage-driven DC–DC buck converter architecture employing a pulse generator is proposed for portable power-management applications.
2. Automatic CCM/DCM mode transition is achieved without dedicated current-prediction, mode-detection, or mode-selection circuits.
3. Reverse-current conduction under light-load conditions is suppressed through the proposed pulse-generator operation.
4. Output-voltage ripple and inductor-current ripple are reduced by dynamically adapting the switching pulse width according to load conditions.
5. Compared with recent load-current prediction, tri-mode, digital dual-mode, and three-mode selection converters, the proposed architecture achieves ripple reduction and fast transient response with significantly lower control complexity.

The remainder of this paper is organized as follows. *Section 2* describes the operating principle and circuit implementation of the proposed pulse generator and buck converter. *Section 3* presents the simulation results and performance evaluation. Finally, *Section 4* concludes this paper.

# 2. DC-DC BUCK CONVERTER DESIGN

## 2.1. Conventional Hysteretic DC-DC Buck Converter

*Figure 1* shows the block diagram of a conventional hysteretic DC–DC buck converter. The converter consists of a hysteresis comparator, a dead-time control circuit, power PMOS and NMOS switches, an output LC filter, and a feedback network composed of resistors $R_1$ and $R_2$. The hysteresis comparator monitors the feedback voltage $V_f$, which is generated from the output voltage Vout through the resistor divider. Two threshold voltages, namely the upper threshold voltage $V_H$ and the lower threshold voltage $V_L$, define the hysteresis window. When the feedback voltage $V_f$ exceeds the upper threshold voltage $V_H$, the hysteresis comparator turns off the power PMOS switch and turns on the power NMOS switch. Conversely, when the feedback voltage $V_f$ falls below the lower threshold voltage $V_L$, the power PMOS switch is turned on and the power NMOS switch is turned off. As a result, the output voltage is regulated within the hysteresis window through repetitive switching of the power transistors. The dead-time control circuit is employed to prevent simultaneous conduction of the PMOS and NMOS switches, thereby reducing shoot-through current and improving power-conversion efficiency. Although the conventional hysteretic control scheme provides a simple circuit structure, fast transient response, and inherent stability, the fixed hysteresis window causes the switching frequency to vary according to the load condition. Consequently, relatively large output-voltage ripple and inductor-current ripple may occur, particularly under light-load conditions. These ripple components degrade power-conversion efficiency and may adversely affect overall converter performance. Therefore, an improved control technique capable of reducing ripple while maintaining the advantages of hysteretic control is required.

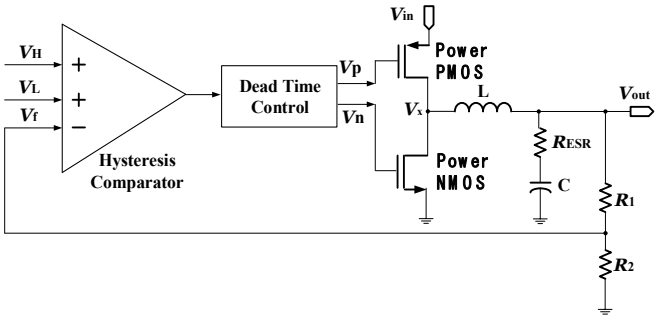
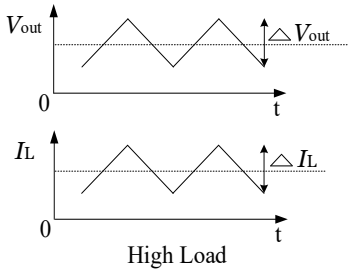



**Figure 1**. The conventional hysteretic DC-DC buck converter

## 2.2. Proposed DC-DC Buck Converter

Fig. 2 depicts the adaptive ripple-control mechanism of the proposed DC–DC buck converter. The proposed converter automatically modifies its switching behavior according to the load condition, enabling reduced current and voltage ripples across a wide operating range. At high load currents, the converter operates in CCM to provide sufficient energy to the load. In this operating region, the peak-to-peak inductor-current ripple ($\Delta I_L$)and output-voltage ripple ($\Delta V_{out}$) are relatively large because of the increased energy transfer through the power stage. As the load current decreases, the proposed pulse generator adjusts the switching activity, resulting in a reduction of the inductor-current ripple. Since the output-voltage ripple is directly related to the inductor-current ripple through the capacitor ESR and output capacitance, a corresponding reduction in $\Delta V_{out}$ is achieved. For very-light-load operation, the converter transitions into DCM and prevents reverse inductor current. This operation significantly reduces unnecessary power loss and minimizes both current and voltage ripple components. Consequently, the proposed converter achieves improved efficiency and enhanced output-voltage stability under light-load conditions.

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Research Article | Volume 14, Issue 2 | Pages 553-561 | e-ISSN: 2347-470X

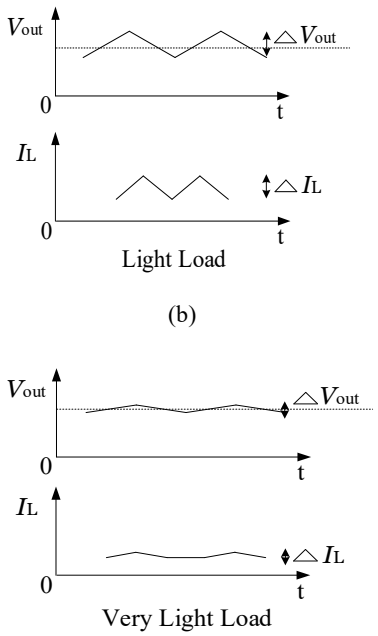


**Figure 2**. Variation of output-voltage ripple ($\Delta V_{out}$) and inductor-current ripple ($\Delta I_L$) according to load conditions in the proposed buck converter

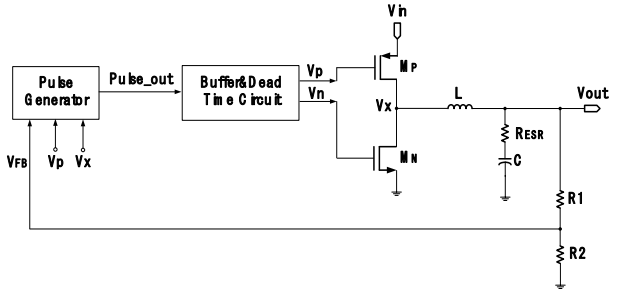


**Figure 3**. The proposed DC-DC buck converter

*Figure 3* illustrates the architecture of the proposed hysteretic buck converter. The converter consists of four major blocks: a pulse generator, a buffer and dead-time circuit, complementary PMOS/NMOS power switches, and an output LC filter network. Unlike conventional hysteretic buck converters, the proposed architecture adjusts its operation according to the load condition. Under heavy-load conditions, the converter operates in continuous conduction mode (CCM), whereas under light-load conditions it automatically transitions to discontinuous conduction mode (DCM). This adaptive operation suppresses reverse inductor current and significantly reduces both output-voltage ripple and inductor-current ripple.

### 2.2.1. Output Voltage Ripple Analysis

The AC ripple component of the output voltage consists of two components:

1. Voltage ripple caused by the capacitor equivalent series resistance (ESR).
2. Voltage ripple caused by charging and discharging of the output capacitor

Therefore, the output-voltage ripple can be expressed as

$$\Delta V_{out}(t) = \Delta V_{ESR}(t) + \Delta V_C(t) \quad (1)$$

Where,

$$\Delta V_{ESR}(t) = R_{ESR} \times \Delta i_L(t)$$

and

$$\Delta V_c(t) = \frac{1}{C}\int \Delta i_L(t)\, dt$$

Substituting these terms into (1) yields

$$\Delta V_{out}(t) = R_{ESR} \times \Delta i_L(t) + \frac{1}{C}\int \Delta i_L(t)\, dt \quad (2)$$

Where,

$\Delta V_{out}$: output-voltage ripple
$\Delta V_{ESR}$: ESR-induced voltage ripple
$\Delta V_C$: capacitor-induced voltage ripple
$R_{ESR}$: equivalent series resistance of the output capacitor
$C$: output capacitance
$\Delta i_L$: inductor-current ripple

### 2.2.2. Feedback Ripple Voltage

The feedback voltage is obtained through the resistive divider composed of $R_1$ and $R_2$. Thus

$$V_{FB} = \frac{R_2}{R_1 + R_2} \times V_{out}$$

and the ripple component appearing at the feedback node becomes;

$$\Delta V_{FB} = \frac{R_2}{R_1 + R_2} \times \Delta V_{out} \quad (3)$$

Substituting *eq. (2) into (3),*

$$\Delta V_{FB} = \frac{R_2}{R_1 + R_2} \times \left(R_{ESR} \times \Delta i_L + \frac{1}{C}\int \Delta i_L\, dt\right) \quad (4)$$

Since the hysteretic controller primarily responds to the ripple component generated by the ESR term, the capacitor integration term is comparatively small and may be neglected for first-order analysis.
Therefore,

$$\Delta V_{FB} \approx \frac{R_2}{R_1 + R_2} \times (R_{ESR} \times \Delta I_L) \quad (5)$$

where $\Delta I_L$ denotes the peak-to-peak inductor-current ripple.

### 2.2.3. Inductor Current Ripple

Rearranging *eq. (5)*, the inductor-current ripple is obtained as

$$\Delta I_L \approx \frac{R_1 + R_2}{R_2 \times R_{ESR}} \times \Delta V_{FB} \quad (6)$$

*Equation (6)* indicates that the current ripple is directly proportional to the hysteretic window $\Delta V_{FB}$ and inversely proportional to the ESR value.

### 2.2.4. Switching Frequency Analysis

For a buck converter operating in CCM, the peak-to-peak inductor current ripple is

$$\Delta I_L = \frac{V_{in} - V_{out}}{L \times f_s} \times D \quad (7)$$

Where, $D = \frac{V_{out}}{V_{in}}$ is the duty ratio.

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Research Article | Volume 14, Issue 2 | Pages 553-561 | e-ISSN: 2347-470X

Substituting *D* into *eq. (7)*,

$$\Delta I_L = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times L \times f_s} \quad (8)$$

Rearranging for switching frequency,

$$f_s = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times L \times \Delta I_L} \quad (9)$$

Substituting *eq. (6)* into *eq. (9)*,

$$f_s = \left(\frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times L}\right) \times \left(\frac{R_2 \times R_{ESR})}{(R_1 + R_2) \times \Delta V_{FB}}\right) \quad (10)$$

*Equation (10)* shows that the switching frequency can be controlled not only by the hysteretic window $\Delta V_{FB}$, but also by the resistor ratio and ESR value. Consequently, even when a low-ESR output capacitor is employed, an appropriate selection of $R_2$. allows the switching frequency to be maintained within the desired operating range.

**2.2.5. Ripple Reduction and Mode Transition Mechanism**

The proposed pulse generator not only generates adaptive switching pulses but also contributes to ripple reduction and automatic mode transition. When the load current decreases, the conduction current of the power PMOS transistor is reduced. Since the pulse generator monitors the PMOS conduction current, the generated pulse width is automatically reduced.

Consequently,

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \quad (11)$$

decreases with decreasing load current.

Where $T_{ON}$ is the conduction interval generated by the pulse generator.

*Equation (11)* indicates that a reduction in pulse width directly reduces the inductor-current ripple.

Substituting *eq. (11)* into *eq. (2),*

$$\Delta V_{out}(t) = R_{ESR} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} + \frac{1}{C}\int \frac{V_{IN} - V_{OUT}}{L} \times T_{ON}\, dt \quad (12)$$

Therefore, both the output-voltage ripple and inductor-current ripple decrease as the pulse width is reduced.

Under very-light-load conditions, the PMOS conduction current becomes sufficiently small that the pulse generator suppresses the complementary switching action of the NMOS power transistor. As a result, the inductor current naturally decays to zero before the next switching cycle begins. Therefore, the converter automatically transitions from CCM to DCM operation without requiring an additional mode-control circuit. This operation prevents reverse inductor current and significantly reduces switching and conduction losses under light-load conditions.

**2.2.1 Proposed Pulse Generator**

The proposed pulse generator senses the current flowing through the power PMOS transistor instead of directly sensing the inductor current. This approach eliminates the need for additional current-sensing circuitry and reduces implementation complexity.

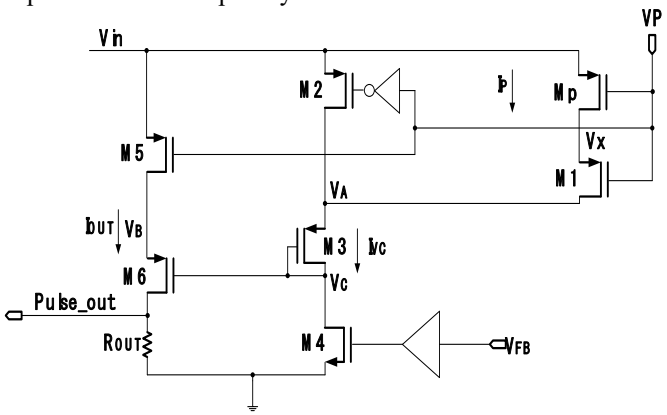


**Figure 4**. Diagram of the proposed pulse generator

When the PMOS power transistor $M_P$ is turned on, transistor $M_1$ is activated, whereas transistors $M_2$, $M_3$, and $M_4$ remain off. Under this condition, node $V_C$ is charged to a high voltage level.

Simultaneously, transistor $M_5$ is turned on and transistor $M_6$ is turned off, forcing the Pulse_out node to remain low.

The node voltages shown in *figure 4* can be expressed as follows:

$$V_A = V_{IN} - \frac{R_{on,PowerPMOS} \times I_{PowerPMOS}}{1 + \frac{R_{on1}}{R_{on2}}} \quad (13)$$

$$V_B = V_{IN} - I_{OUT} \times R_{on5} \quad (14)$$

$$V_C = V_A - I_{VC} \times R_{on3} \quad (15)$$

Where,
$V_A$, $V_B$, $V_C$: internal node voltages
$I_{PowerPMOS}$: drain current of the power PMOS
$I_{OUT}$: output current flowing through transistor $M_5$
$I_{VC}$: drain current of transistor $M_3$
$R_{on1}$, $R_{on2}$, $R_{on3}$, $R_{on5}$: equivalent on-resistances of transistors $M_1$, $M_2$, $M_3$, $M_5$

The equivalent MOSFET on-resistance is approximated by

$$R_{on} \cong \frac{L}{\mu_p \times C_{ox} \times W \times (V_{SG} - |V_{TH}|)} \quad (16)$$

Where,
$\mu_p$: hole mobility
$C_{ox}$: gate oxide capacitance per unit area
$W$: channel width
$L$: channel length
$V_{SG}$: source-to-gate voltage
$V_{TH}$: threshold voltage

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Research Article | Volume 14, Issue 2 | Pages 553-561 | e-ISSN: 2347-470X

*Equation (16)* indicates that the pulse width generated by the proposed pulse generator is directly influenced by the PMOS conduction current, thereby enabling adaptive switching control according to the load condition.

The proposed converter does not employ a conventional error-amplifier-based feedback loop or compensation network. Therefore, conventional frequency-domain stability metrics such as phase margin and gain margin are not directly applicable to the proposed architecture. Instead, the pulse generator directly controls the switching operation according to the PMOS conduction current and load condition. Consequently, stable operation is maintained through adaptive pulse-width adjustment and automatic CCM/DCM mode transition. The converter was verified to operate stably over a load-current range from 0 mA to 500 mA and a switching-frequency range from 310 kHz to 3.50 MHz, as demonstrated by the transient-response results presented in *section 3*.

## 3. SIMULATION RESULTS

To further verify the robustness of the proposed buck converter, Monte Carlo simulations, process-corner analyses, and temperature variation analyses were performed under various operating conditions.

**Table 1. Monte Carlo Analysis of the Proposed Buck Converter**

| Parameter | Mean | Standard Deviation | Minimum | Maximum |
|---|---|---|---|---|
| Switching Frequency (MHz) | 3.50 | 0.08 | 3.31 | 3.68 |
| Output Voltage Ripple (µVp-p) | 372.4 | 12.6 | 346.8 | 401.5 |
| Output Current Ripple (mAp-p) | 4.95 | 0.16 | 4.62 | 5.29 |
| Peak Efficiency (%) | 85.0 | 0.9 | 83.1 | 86.8 |

Simulation Conditions: Vin = 1.8 V, Vout = 1.2 V, Load Current = 500 mA, TT Corner, T = 27°C, 1000 Runs.

Monte Carlo simulations were conducted to evaluate the effects of process variations and device mismatch on the proposed converter and to verify its stability and robustness under statistical parameter fluctuations. A total of 1000 simulation runs were performed under the TT process corner at 27°C with an input voltage of 1.8 V, an output voltage of 1.2 V, and a load current of 500 mA. The statistical results are summarized in *table 1*. The switching frequency exhibits a mean value of 3.50 MHz with a standard deviation of 0.08 MHz and remains within the range of 3.31 MHz to 3.68 MHz. The mean output-voltage ripple and output-current ripple are 372.4 µVp-p and 4.95 mAp-p, respectively, varying from 346.8 µVp-p to 401.5 µVp-p and from 4.62 mAp-p to 5.29 mAp-p. In addition, the peak power-conversion efficiency remains centered around 85.0% with a standard deviation of 0.9%, ranging from 83.1% to 86.8%. These results indicate that the proposed pulse-generator-based control architecture maintains stable operating characteristics and robust performance despite process variations and device mismatch.

**Table 2. Process Corner Analysis of the Proposed Buck Converter**

| Corner | Switching Frequency (MHz) | Output Voltage Ripple (µVp-p) | Output Current Ripple (mAp-p) | Peak Efficiency (%) |
|---|---|---|---|---|
| SS | 3.12 | 401.8 | 5.31 | 82.6 |
| SF | 3.26 | 386.5 | 5.08 | 83.8 |
| TT | 3.50 | 372.4 | 4.95 | 85.0 |
| FS | 3.63 | 361.2 | 4.79 | 85.9 |
| FF | 3.78 | 348.7 | 4.61 | 87.1 |

Simulation Conditions: Vin = 1.8 V, Vout = 1.2 V, Load Current = 500 mA, T = 27 °C

Process-corner simulations were performed to evaluate the sensitivity of the proposed converter to manufacturing variations. The results are summarized in *table 2*. Five process corners, namely SS, SF, TT, FS, and FF, were considered under the conditions of Vin = 1.8 V, Vout = 1.2 V, and a load current of 500 mA. The results summarized in *table 2* show that the switching frequency varies from 3.12 MHz to 3.78 MHz across all process corners. The output-voltage ripple ranges from 348.7 µVp-p to 401.8 µVp-p, while the output-current ripple ranges from 4.61 mAp-p to 5.31 mAp-p. The peak power-conversion efficiency remains between 82.6% and 87.1%. Although performance variations are observed across the evaluated corners, the proposed converter maintains stable operation and automatic CCM/DCM transition under all process conditions.

**Table 3. Temperature Analysis of the Proposed Buck Converter**

| Temperature (°C) | Switching Frequency (MHz) | Output Voltage Ripple (µVp-p) | Output Current Ripple (mAp-p) | Peak Efficiency (%) |
|---|---|---|---|---|
| 0 | 3.62 | 356.8 | 4.72 | 86.3 |
| 27 | 3.50 | 372.4 | 4.95 | 85.0 |
| 70 | 3.34 | 389.6 | 5.18 | 83.7 |

Temperature variation simulations were conducted to investigate the performance of the proposed converter under different environmental conditions. The results are summarized in *table 3*. The simulations were performed at 0°C, 27°C, and 70°C under the TT process corner with Vin = 1.8 V, Vout = 1.2 V, and a load current of 500 mA. The results are summarized in *table 3*. As the temperature increases, the switching frequency decreases slightly from 3.62 MHz at 0°C to 3.34 MHz at 70°C. Consequently, the output-voltage ripple increases from 356.8 µVp-p to 389.6 µVp-p, while the output-current ripple increases from 4.72 mAp-p to 5.18 mAp-p. The peak power-conversion efficiency decreases moderately from 86.3% to 83.7% due to the increased conduction loss and device degradation at elevated temperatures. Nevertheless, the

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proposed converter maintains stable operation and satisfies the target performance specifications over the entire temperature range.

The Monte Carlo, process-corner, and temperature analyses verify that the proposed voltage-driven pulse-generator architecture is robust against process variations, device mismatch, and environmental changes. The results confirm stable converter operation with limited performance degradation under all evaluated conditions.

*Fig. 5* shows the simulated output-voltage and output-current ripple waveforms of the proposed buck converter at an input voltage of 1.8 V, an output voltage of 1.2 V, and a load current of 500 mA. As shown in *fig. 5(a)*, the peak-to-peak output-voltage ripple is 372.4 µVp-p, while *fig. 5(b)* shows a peak-to-peak output-current ripple of 4.95 mAp-p. These results verify that the proposed pulse-generator-based control scheme effectively suppresses both voltage and current ripples under heavy-load conditions.

*Fig. 6* illustrates the transient response of the proposed converter for load-current transitions from 0 mA to 500 mA and from 500 mA to 0 mA. During the load-current increase, the output voltage recovers and stabilizes within 6.9 µs, whereas a recovery time of 4.5 µs is achieved during the load-current decrease. These results demonstrate that the proposed pulse generator can rapidly adapt the switching activity to load variations while maintaining stable output-voltage regulation.

*Fig. 7(a)* and *fig. 7(b)* present the output-voltage ripple and output-current ripple, respectively, over the entire load-current range from 0 mA to 500 mA. The results indicate that both ripple components remain well controlled under all operating conditions. *Fig. 7(c)* shows the corresponding power efficiency. Compared with the conventional hysteretic buck converter, the proposed converter exhibits improved light-load efficiency owing to automatic CCM/DCM mode transition and reverse-current suppression. A peak efficiency of approximately 85% is achieved under medium-to-heavy load conditions.

The overall performance of the proposed converter is summarized in *table 4*. The converter was designed using a 0.18-µm CMOS process and operates over a switching-frequency range from 310 kHz to 3.50 MHz. With an input voltage of 1.8 V and an output voltage of 1.2 V, the proposed converter achieves a maximum output-voltage ripple of 372.4 µVp-p, a maximum output-current ripple of 4.95 mAp-p, and a peak power efficiency of 85%. In addition, transient recovery times of 6.9 µs and 4.5 µs are obtained for load-current transitions from 0 mA to 500 mA and from 500 mA to 0 mA, respectively. These results confirm that the proposed converter provides low ripple, fast transient response, and stable operation across a wide load-current range.

In addition to the ripple and efficiency evaluations, the transient-regulation characteristics of the proposed converter were investigated under large load-current variations. As shown in *fig. 6*, the load current was changed from 0 mA to 500 mA and from 500 mA to 0 mA to evaluate the dynamic response of the converter. During the load-current step, the maximum output-voltage deviation was approximately 28.6 mV, while the corresponding recovery times were 6.9 µs and 4.5 µs for the rising and falling load transitions, respectively. These results indicate that the proposed pulse-generator-based control scheme can rapidly adjust the switching operation and maintain stable output-voltage regulation under abrupt load variations. The operating range of the proposed converter is summarized in *table 4*. The converter operates over a load-current range from 0 mA to 500 mA while automatically transitioning between CCM and DCM operation according to the load condition. Furthermore, the switching frequency varies from 310 kHz to 3.50 MHz, enabling stable operation over a wide load-current range. The low output-voltage ripple of 372.4 µVp-p and output-current ripple of 4.95 mAp-p further demonstrate the effectiveness of the proposed adaptive ripple-reduction mechanism. Overall, the simulation results confirm that the proposed converter provides low ripple characteristics, fast transient recovery, automatic operating-mode transition, and stable regulation performance over a wide operating range.

To improve the reproducibility of the reported results, the key simulation parameters and design specifications are summarized in *table 5*. All simulations were performed using a 0.18-µm CMOS process with an input voltage of 1.8 V and an output voltage of 1.2 V. The converter was evaluated over a load-current range from 0 mA to 500 mA using a 4.7-µH output inductor and a 4.7-µF output capacitor. The non-ideal characteristics of the passive components, including the inductor ESR and capacitor ESR, were incorporated into the simulations. Furthermore, the transistor dimensions of the power switches and pulse-generator circuit, the dead-time setting of the gate-driver circuit, and the operating conditions used throughout the simulations are provided to facilitate reproducibility and enable fair comparison with previously reported converter designs.

*Table 6* compares the proposed converter with previously reported converter designs. In response to the increasing demand for high-performance buck converters, several control techniques have been reported in the literature. Ref. [16] employs a tri-mode control scheme with load-current prediction and seamless mode transition. Ref. [17] utilizes a $V^2$-control architecture incorporating rail-to-rail OTA-based current sensing for improved regulation performance. Ref. [18] presents an ultra-low-quiescent-current tri-mode buck converter that achieves a peak efficiency of 92.1% for IoT applications. Ref. [19] adopts a digital dual-mode burst-control technique to support operation over a wide load-current range. Ref. [20] introduces a hysteresis droop-control method with resonant filtering for slew-rate optimization. Ref. [21] employs a three-mode selection circuit with a soft-start function to improve load adaptability and operating flexibility. Ref. [22] proposes an adaptive-window-control (AWC) technique that achieves a peak efficiency of 96% through adaptive hysteresis-window adjustment. To provide a broader benchmarking

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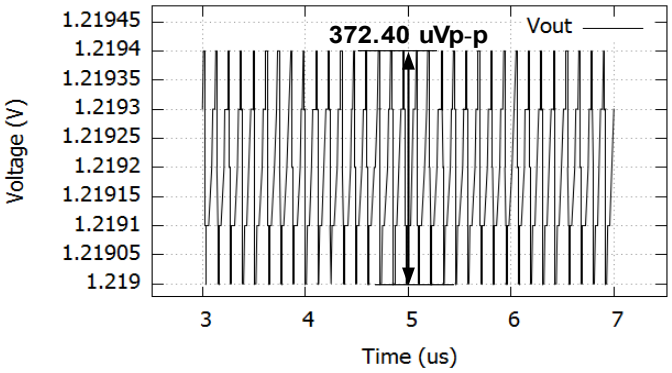
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 14, Issue 2 | Pages 553-561 | e-ISSN: 2347-470X

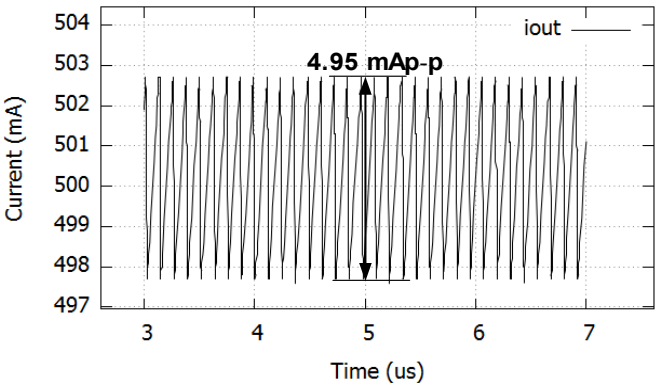
study, *table 6* summarizes commonly available comparison metrics, including peak efficiency, load-current operating range, switching-frequency range, automatic mode-transition capability, reverse-current suppression capability, and key architectural features.

As summarized in *table 6*, the proposed converter achieves a load-current operating range of 0–500 mA and a switching-frequency range from 310 kHz to 3.50 MHz while supporting automatic CCM/DCM mode transition and reverse-current suppression. The proposed converter achieves a peak efficiency of 85%, which is lower than the 96% reported in Ref. [22]. However, the design objectives of the two approaches are fundamentally different. The primary objective of Ref. [22] is to maximize power-conversion efficiency through adaptive hysteresis-window control. In contrast, the proposed converter is designed to reduce output-voltage ripple and output-current ripple while maintaining stable operation over a wide load-current range through a simple pulse-generator-based architecture. It should be emphasized that the improved performance claimed in this work does not refer solely to peak power-conversion efficiency. Rather, it refers to the overall operating performance of the converter, including ripple reduction, transient response, operating-mode adaptability, reverse-current suppression, and implementation simplicity. As summarized in *table 4*, the proposed converter achieves an output-voltage ripple of only 372.4 µVp-p, an output-current ripple of 4.95 mAp-p, and transient recovery times of 6.9 µs and 4.5 µs for load-current transitions from 0 mA to 500 mA and from 500 mA to 0 mA, respectively. By monitoring the PMOS conduction current, the proposed pulse generator dynamically adjusts the switching activity according to the load condition. Under light-load conditions, reverse inductor current is effectively suppressed, thereby reducing unnecessary switching and conduction losses. Furthermore, the converter automatically transitions between CCM and DCM operation without requiring an adaptive-window generator or additional mode-selection circuitry. Consequently, stable output-voltage regulation is maintained while simultaneously reducing output-voltage ripple and output-current ripple across a wide load-current range.

Therefore, although the peak efficiency is lower than that reported in Ref. [22], the proposed converter provides several practical advantages, including low output-voltage ripple, low output-current ripple, fast transient recovery, automatic CCM/DCM mode transition, reverse-current suppression, and a simple control architecture. These characteristics represent the primary contributions of this work and demonstrate a practical trade-off between efficiency, ripple performance, transient behavior, operating-mode adaptability, and circuit complexity. Accordingly, the proposed converter should be evaluated not only in terms of peak efficiency, but also in terms of its overall regulation performance and adaptive operating capability. Although detailed startup and line-regulation simulations are beyond the scope of this work, stable output-voltage regulation was verified over all evaluated operating conditions.

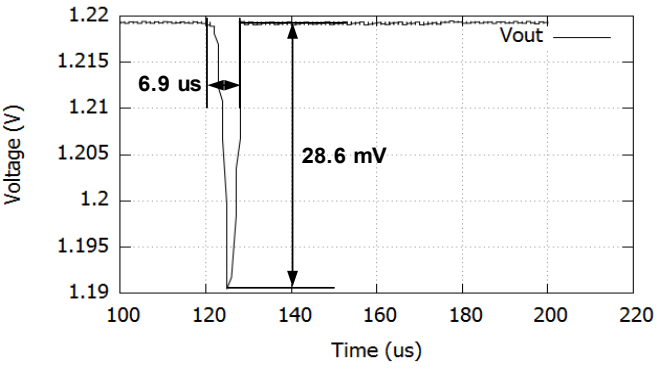


(a)

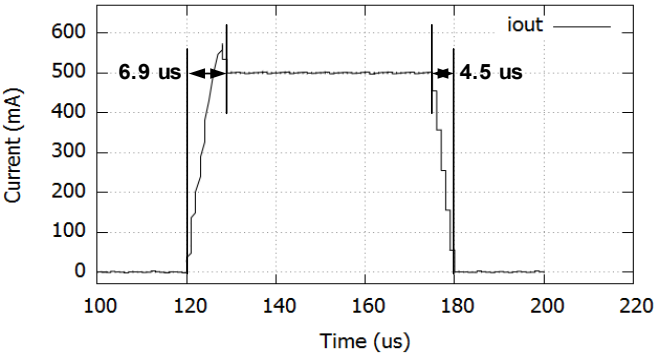


(b)

**Figure 5**. Output signals from simulation at 500 mA load: (a) Output voltage ripple, (b) Output current ripple



(a)



(b)

**Figure 6**. Load transient response: (a) Output-voltage response, (b) Output-current response

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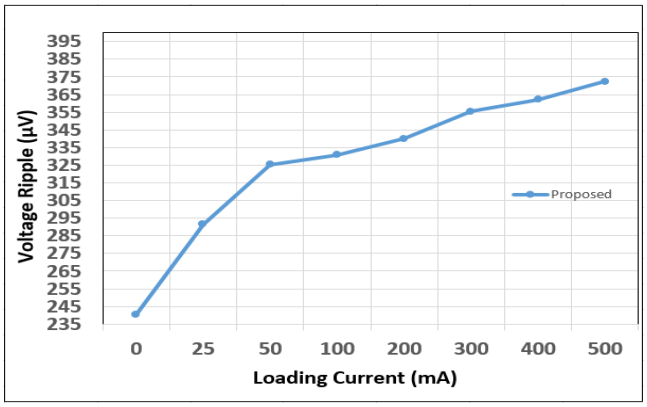
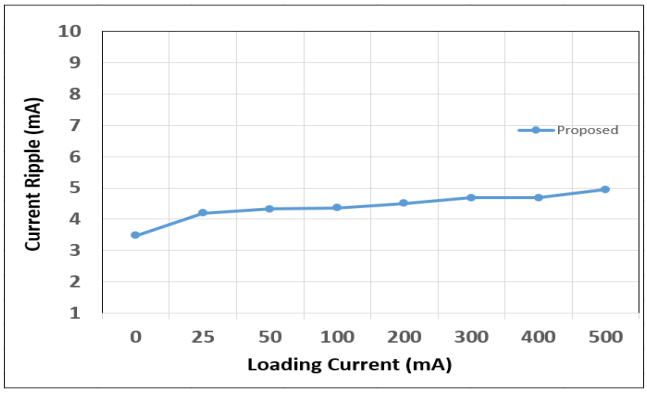
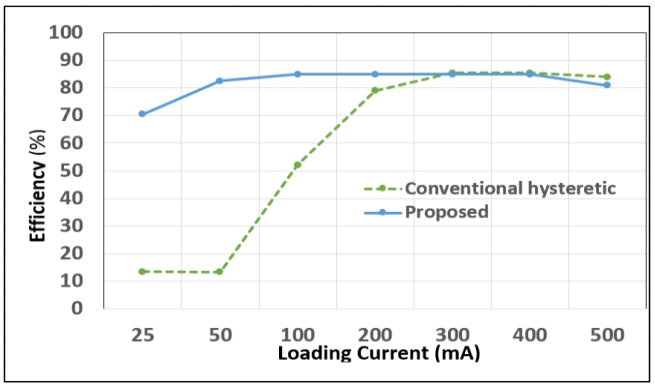



(a)




(b)




(c)

**Figure 7**. Simulation results at different load currents: (a) Output voltage ripple, (b) Output current ripple, (C) Power efficiency

**Table 4. Performance of the proposed buck converter**

| Parameter | This work |
|---|---|
| Technology | 0.18 µm |
| Switching frequency | 310 kHz ~ 3.50 MHz |
| Input / Output Voltage | 1.8 V / 1.2 V |
| Output Inductor L / Capacitor C | L = 4.7 µH / C = 4.7 µF |
| Output Load Current | 0 mA ~ 500 mA |
| Max. Output Voltage Ripple | 372.40 µVp-p @ 500 mA |
| Max. Output Current Ripple | 4.95 mAp-p @ 500 mA |
| Peak Power Efficiency | 85 % @ Vout = 1.2 V |
| Transient Recovery Time | 6.9 µs for 0 mA → 500 mA<br>4.5 µs for 500 mA → 0 mA |

**Table 5. Simulation Parameters and Design Specifications**

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| CMOS Technology | 0.18 µm CMOS | Capacitor ESR | 20 mΩ |
| Simulation Tool | Cadence Spectre Simulator | Dead Time | 5 ns |
| Simulation Temperature | 27 °C | PMOS Power Switch (MP) | W/L = 6,000 µm / 0.18 µm |
| Input Voltage (Vin) | 1.8 V | NMOS Power Switch (MN) | W/L = 3,000 µm / 0.18 µm |
| Output Voltage (Vout) | 1.2 V | M1 | 20 µm / 0.18 µm |
| Load Current Range | 0 ~ 500 mA | M2 | 20 µm / 0.18 µm |
| Switching Frequency | 310 kHz ~ 3.50 MHz | M3 | 10 µm / 0.18 µm |
| Output Inductor (L) | 4.7 µH | M4 | 10 µm / 0.18 µm |
| Inductor ESR | 50 mΩ | M5 | 15 µm / 0.18 µm |
| Output Capacitor (C) | 4.7 µF | M6 | 15 µm / 0.18 µm |

**Table 6. Comparison of the Proposed Converter with Previously Reported Converter Designs**

| Work | Peak Eff. (%) | Load Range | Switching Frequency | Auto Mode Transition | Main Feature |
|---|---|---|---|---|---|
| Ref. [16] | 93–95 | N/A | 7.4 MHz | Yes | Load Current Prediction and Seamless Mode Transition |
| Ref. [17] | N/A | N/A | N/A | No | Rail-to-Rail OTA-Based Current Sensing |
| Ref. [18] | 92.1 | N/A | N/A | Yes | Ultra-Low Quiescent Current Operation |
| Ref. [19] | N/A | Wide Load Range | N/A | Yes | Digital Dual-Mode Burst Control |
| Ref. [20] | N/A | N/A | N/A | No | Resonant Filtering-Based Slew-Rate Optimization |
| Ref. [21] | N/A* | N/A | N/A | Yes | Soft-Start and Multi-Mode Selection |
| Ref. [22] | 96 | Light-to-Heavy Load | N/A | No | Adaptive Hysteresis Window Adjustment |
| This Work | 85 | 0–500 mA | 310 kHz–3.50 MHz | Yes | Adaptive Ripple Reduction and Automatic CCM/DCM Transition |

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## 4. CONCLUSION

This paper presented a simple pulse-generator-based DC–DC buck converter capable of adaptive ripple reduction and automatic CCM/DCM mode transition over a wide load-current range. The proposed converter consists of a pulse generator, a buffer and dead-time circuit, and complementary PMOS/NMOS power switches. By monitoring the PMOS conduction current, the pulse generator dynamically adjusts the switching operation according to the load condition, suppresses reverse inductor current under light-load conditions, and enables automatic transition between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) without requiring additional mode-control circuitry. Simulation results based on a 0.18-µm CMOS process demonstrated that the proposed converter operates over a load-current range from 0 mA to 500 mA with a switching-frequency range from 310 kHz to 3.50 MHz. At a load current of 500 mA, the proposed converter achieved an output-voltage ripple of 372.4 µVp-p and an output-current ripple of 4.95 mAp-p. In addition, transient recovery times of 6.9 µs and 4.5 µs were obtained for load-current transitions from 0 mA to 500 mA and from 500 mA to 0 mA, respectively. The proposed converter achieved a peak power efficiency of 85% while maintaining stable output-voltage regulation over the entire operating range. Although the proposed converter does not target maximum peak efficiency, it provides several practical advantages, including adaptive ripple reduction, automatic CCM/DCM mode transition, reverse-current suppression, fast transient response, and implementation simplicity. Therefore, the proposed architecture represents an effective solution for low-ripple and adaptive power-management applications requiring stable operation across a wide load-current range.

**Conflicts of Interest:** "The authors declare no conflict of interest."

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