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Design and Simulation of QCA-based 4:1 Multiplexer: Energy Dissipation and Fault Tolerance Analysis

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ABSTRACT- Quantum Dot Cellular Automata has arisen as a promising nanotechnology for the enactment of high-density and ultra-low power digital circuits beyond conventional CMOS Technology. In this exertion a 4:1 QCA-based Multiplexer is designed using region-based interaction methodology and four-phase clocking scheme. The proposed design utilizes total 45 cells with area occupancy of 0.006 μm^2 with latency of one clock cycle. To authenticate the design methodology, an alternative 40-cell layout design for 4:1 Multiplexer was also implemented so as to confirm the precision of the methodology. Simulation and functional verification were executed by using QCA Designer 2.0.3, while energy dissipation analysis was carried out using QCA Designer-E under Coherence Vector Energy Simulation engine at an operating Temperature of 1K by exploiting both Euler's and Runge-Kutta Method numerical methods. The proposed design exhibits a total energy dissipation of 1.62×10^{-2} eV and an Average energy dissipation of 1.48×10^{-3} eV per cycle using Euler's Method while Runge-Kutta Method reports total energy dissipation of 1.74×10^{-2} eV and average energy dissipation of 1.58×10^{-3} eV per cycle. The designed layout attained a cell omission tolerance of 66.67%, while misalignment analysis confirmations functional rates of 87.5%,87.5% and 75% for displacement values of 5nm,10nm, and 15nm. Furthermore, the correlation between kink energy and fault tolerance executed in this work confirms that regions with stronger electrostatic coupling exhibit improved robustness against fabrication-induced defects. Comparative analysis also shows better improvement in terms of energy dissipation and other performance parameters as compared to existing multiplexer designs, which indicates the suitability of the proposed architecture for reliable nanoscale QCA implementations.

Keywords: Quantum Dot Cellular Automata, Multiplexer; Energy Dissipation, Euler's Method, Runge Kutta Method, Fault Tolerance, Kink Energy, Polarization Energy.

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1. INTRODUCTION

The incessant scaling of conventional CMOS technology required the rapid progression for designing of digital circuits with compact area and less energy dissipation. However, as the transistor dimensions penetrate sub-micron thresholds such as 45nm, physical constrains deliver unembellished restrictions using CMOS based designs [1]. The several confines needed to overcome in conventional CMOS designs comprised Quantum effects, extreme lithographic needs, severe leakage currents, and thermal dissipation. Consequently, there is requirement for nano-based designs for having alternative nanoscale, transistor-less designs and the expertise that offer high operational density and ultra-low power consumption. There are several state-of-the-art technologies that are able to deliver a highly feasible and revolutionary substitute to overcome scaling confines of CMOS from where QCA i.e. Quantum Dot Cellular Automata is emerging is highly promising. In Quantum Dot Cellular Automata the circuit are premeditated by the use of QCA cells which operates on principle of electrostatic interactions among the coupled quantum-dots present in QCA cell rather than electric current flow [2]. Therefore, QCA cells represent binary states *i.e.* Binary '0' and Binary '1' through electron configuration polarization. This approach thus able to eradicates traditional source-to-drain leakage currents and consequently diminishes the thermodynamic energy losses through logic transitions. As a result, implementation of digital routing primitive within QCA corresponding multiplexers which performances as backbone of arithmetic and logic unit (ALU) designs is a critical part of survey [3].

Multiplexers can well-though-out as a foundational subsystem in digital logic design and are responsible for channel selection and data routing. There is persistent prerequisite for reducing design complexity and energy dissipation for designing of a logic primitive like multiplexer in QCA -based designing. The systematic study of earlier literature for QCA-based Multiplexer design reveals clear challenges for designing of MUX. By considering initial designs based on majority-gate mapping they suffer from significant cell count overhead or inhibited wire-crossing routing for auxiliary signal paths. However, QCA-based MUX designs consuming multi-layer framework consequences in large energy dissipation and immense manufacturing complexity due to multi-layer crossover-bridges. In contrast to this single-layer or coplanar restricted Multiplexer designs results in latency and severe propagation delay during sequential routing or complex routing loops largely at higher input counts.

High cell minimization techniques can be executed by means of cell interaction mechanism signal distribution networks further needed high density layout tolerance and high-precision clock isolation so as to avoid signal degradation. Moreover, sustain robust logic polarization within selection interface region deprived of a select line wire crossing remains persistent layout task. To bridge these research gaps, this paper proposed a compact 4:1 Multiplexer Architecture based on bottom-up architectural methodology where is design exploited localized potential-well interaction zones so as to avoid complex wiring crossover and attained compact and single -layer topology. Unlike other designs which demand independent control buses across all blocks, the proposed design architecture that is able to route signal to an interaction node where the terminal selection stage resolve stage selection through localized cell potential minimization against fixed polarization control. The structural integrity of the designed 4:1 MUX is meticulously substantiated using multi-phase clocking scheme from clock 0 to clock 3 so as to deliver data propagation. In this paper, thermal and energy analysis is performed so as to confirm the thermal stability and polarization stability of the designed architecture.

2. LITERATURE SURVEY

The state-of-the-art multiplexers design in Quantum Dot Cellular Automata is primarily focused on minimization of cell counts, active area footprint, and propagation latency. Early architecture designs for QCA-based MUX designs optimized the logical layout from functional perspective. For example, Chabi .et. al [29] employed fundamental design styles so as to construct basic binary routers that confirm stable multi-bit configurations but at the cost of insignificant layout redundancies. Similarly, Ahmadpour [23] developed fault-tolerant multi-bit multiplexers where structural design attained by redundant majority gates for data propagation but this method limit scalability. In order to further lower the layout design area and clock latency researchers employed specialized logical formulations and structural layers. Jeon. et. al [14] minimized the layout area by introducing majority function-based NAND mapping for quantum computing environments. Almatrood et.al. [27] considered low-power structural layouts which target modular digital integration however, Mosleh.et.al [13] and Xingjun.et.al [12] extended upon high-speed multi-bit-data selection blocks consuming conventional layer routing schemes. Recent design methodologies emphasis profoundly on reversible computing and nanoscale physical cell optimization. Pathak.et.al [16] and Ahmad et.al. [26] appraised testable and multibit (2N:1) QCA-based MUX designs that evade crossover but somehow affect latency. Alkaldy.et.al [22], however, optimized the baseline macro blocks for designing of Multiplexers. Alharbi.et.al [28] advanced this scaling standard by synthesizing an ultra-energy-efficient reversible 8:1 Multiplexer design by means of explicit multi-layer frameworks but this procedure somehow upsurge intricacy in the layout design. Finally, state-of-art designs by Bagheri.et.al [15] and Jana.et.al [19] have considerably limit the boundaries by introducing signal distribution networks by lowering typical 4:1 multiplexer layout design near or below 100-cell by ensuring full logical validation but still aspects polarization instability.

3. PROPOSED QCA-BASED 4:1 MUX DESIGN

The proposed QCA-based 4:1 Multiplexer is designed as shown in Fig.1.The designed architecture is composed of three functional regions where the first two regions operate as data local data-selection stages, while the third region performs the final output resolution through QCA cell interactions. The designed architecture employs Majority-gate-based logic and clock-controlled polarization propagation so as to accomplish multiplexing functionality with compact cell count and reduces routing intricacy.

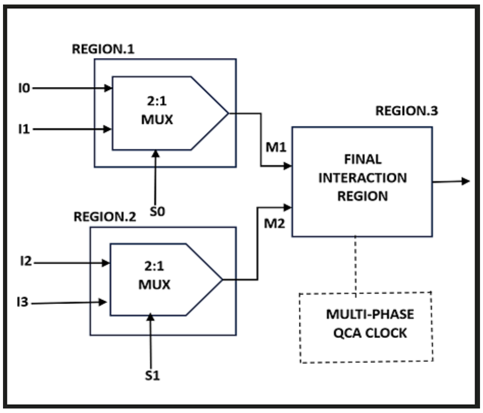

Figure 1. Block Diagram of proposed 4:1 Multiplexer Design

Operation of Region.1

Region.1 behaves as a conventional 2:1 MUX and selects one of the two input signals I_0 and I_1 depending upon select signal S_0. Therefore, the output of region.1 is represented as:

$$M1= \overline{S0}I0+S0I1$$

Therefore, for S_0=0, M_1=I_0 and for S_0=1, M_1=I_1

Operation of Region.2

Similarly, Region.2 acts as a 2:1 MUX and selects one of the two input signals I_2 and I_3. So, in Region.2 the output is expressed as:

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$$M2=\overline{S1}I2 + S1I3$$

Therefore, for S1=0, M2=I2 and for S1=1, M2=I3

Final Interaction Region

The outputs M_1 and M_2 are propagated towards the final interaction region. Unlike conventional cascaded multiplexer structures, this region does not necessitate and explicitly routed final select line. However, the selection information generated in the preceding stages are supported through cell polarizations and resolved through majority-based QCA interactions and clock-controlled signal propagation. The final or third region therefore performances as polarization-resolution stage which combines the conditional outputs from the previous regions and produces the desired multiplexed output.

Functional Verification

The functionality of the complete architecture was verified by applying all possible combinations of select signals S_0 and S_1.

For S_0S_1=00, $Y=I_0$ $\overline{S0}S1 = I1$ $S0\overline{S1}=I_2$ $\overline{S0}\,\overline{S1} = I3$

Therefore, we get resulting Truth Table as:

Table 1. Truth Table of Proposed 4:1 Multiplexer

S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Consequently, we get the output equation as: $Y=\overline{S0S1}I0 + \overline{S0}S1I1 + S0\overline{S1}I2 + S0S1I3$

The derived equation precisely matches the canonical Boolean expression of a standard 4:1 Multiplexer design. Therefore, the anticipated design is mathematically and functionally substantiated. Based on this methodology, the physical layout for 4:1 Multiplexer can be designed by using QCA Designer 2.0.3 with simulation setup as shown in *table 2*. The layout is premeditated within a single layer deprived of any crossover so as to eliminate the manufacturing defects associated with multi-layer wire crossovers.

Table 2. Simulation Setting for QCA Designer 2.0.3

Design Parameter	Description	Value	Unit
Temp (T)	Operating Temperature	1K	K
Dot cell	Quantum Dot Cell size	18nm	Nm
QD size	Quantum Dot diameter size	5nm	Nm
CLK zone	Clock zones	4	Clock cycles
Samples	Total number of samples	12800	
Tolerance	Convergence tolerance	0.001000	
Radius of effect	Maximum distance considered for interactions between cells	65.000000	Nm
Relative Permittivity	Relative permittivity of materials used in QCA systems	12.900000	
Clock High	Maximum saturation energy of clock	9.800000e-022	J
Clock Low	Minimum saturation energy of clock	3.800000e-023	J
Clock amp	Clock amplitude factor	2.000000	Clock cycles
Layer separation	Distance between QCA layers in multilayer crossing	11.500000	Nm
Iterations	Maximum iterations per sample	100	

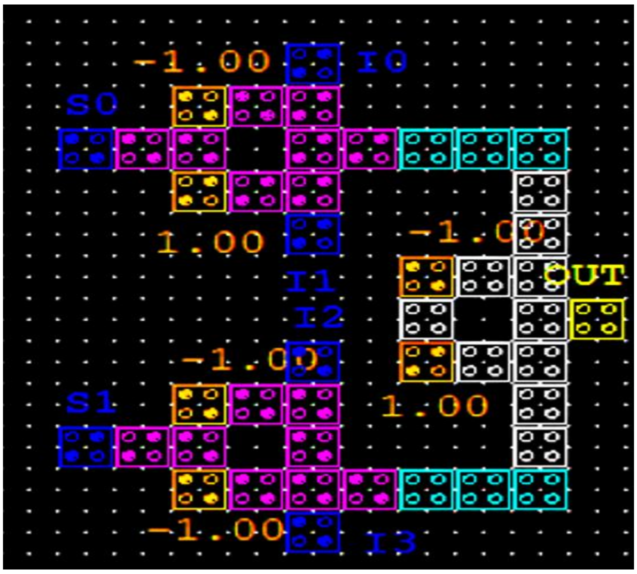

Figure 2. Proposed 4:1 Multiplexer Layout Design

Figure 2 shows the physical implementation of proposed 4:1 Multiplexer in a single layer design structure by using 45 cells and total area of 0.05 µm^2. By mapping the architectural design directly on a coplanar cell matrix, the anticipated design effectively eliminates multi-layer wire crossovers and complex routing pathways. The physical structure of the designed architecture precisely mirrors the three region functional zones that we demarcated in the theoretical analysis. Region.1 is shown as the Top region executed as 2:1 MUX using select line S_0 and input lines I_0 and I_1.Region.2 is shown as the bottom region which likewise working as 2:1 MUX with select line S_1 and input lines I_2 and I_3.Final region Region.3 is shown at right side and is substitute as polarization resolution stage where the intermediate signals M_1 and M_2 converge by cell-to cell Coulombic interactions so as to resolve the final output state *Y* reliant on the incoming states. The proposed layout design utilizes a 4-phase clocking mechanism so as to ensure smooth sequential signal propagation.

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Table 3. Clocking Scheme of Proposed Layout

Region	Dominant Clock
Inputs (S_0, S_1, I_0, I_1, I_2, I_3)	Clock 0
Local Selection Blocks	Clock 1
Propagation Paths	Clock 2
Final Interaction Region	Clock 3
Output Cell	Follows Clock 3 results

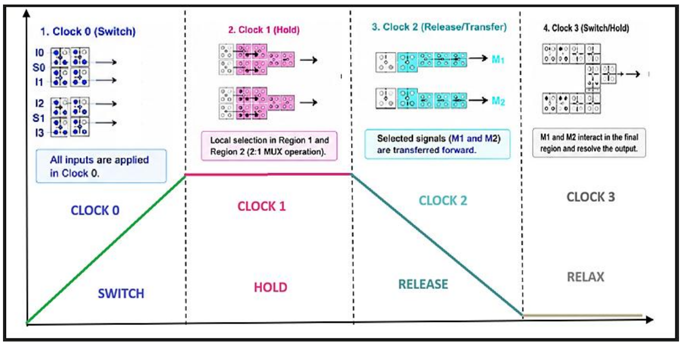

Figure 3. Clocking scheme for proposed design

To validate the proposed design methodology, we implemented another 4:1 Multiplexer of using 40 cells in total with Total area consumption of 0.007µm^2 by using the same polarization interaction concept and four-phase clocking scheme as shown in *figure 4*. Even though the physical arrangement of cells diverges from the primary design, the proposed design.2 efficaciously realizes the standard 4:1 multiplexing function reliant upon the design methodology conferred above. The obtained results confirm that the anticipated design approach can be applied to alternative layouts while preserving correct functionality and thus validating the effectiveness and repeatability of the methodology.

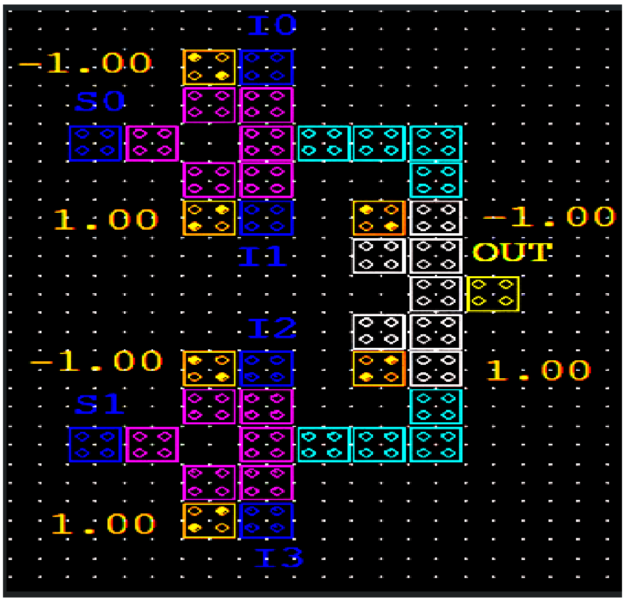

Figure 4. 40-cell 4:1 layout design (Design.2)

4. RESULTS AND PERFORMANCE ANALYSIS

By using the above parameters in QCA Designer 2.0.3 we get the simulation results by using the simulation setup as shown in *table 1*. Simulation waveform shown in *figure 5,6* follow the required truth table of 4:1 multiplexer with output followed to either one of inputs which are I_0, I_1, I_2 and I_3 depending upon the logic combination of select inputs S_0 and S_1. *Figure 5,6* shows simulation waveform with 45 cells and with 40 cells, respectively. Stable polarization levels were pragmatic throughout the simulation which specifies reliable logic propagation without distortion. Both designs accomplish correct logical functionality with a latency of one clock cycle.

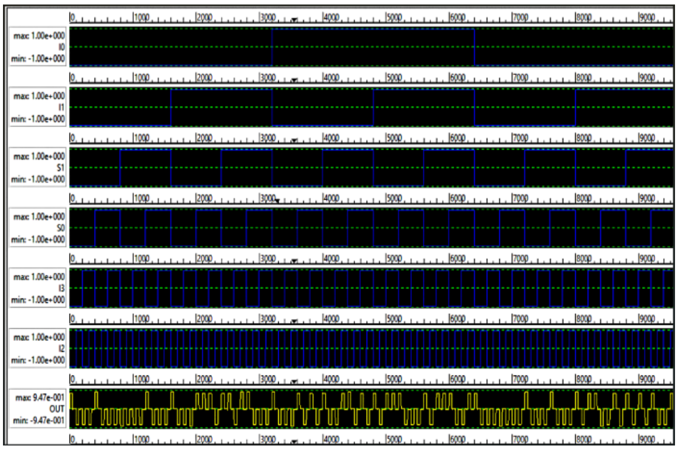

Figure 5. Simulation Waveform for proposed 4:1 Multiplexer

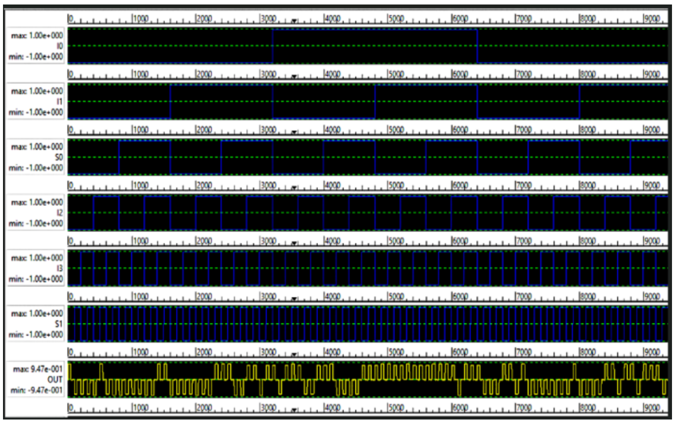

Figure 6. Simulation Waveform for 4:1Multiplexer Design.2

Figure 5 shows the simulation waveform for designed 4:1 QCA -based Multiplexer consuming 45-cells. Here the select line signals S_0 and S_1 control the selection procedure of the corresponding input signals I_0, I_1, I_2, I_3. As the select line signals changes their combinations from 00,01,10,11, the output follows the respective selected input, and therefore confirm the correct realization of the multiplexing function. The resultant waveform shows proper polarization propagation and signal transfer by the use of discussed four-phase clocking scheme. To further corroborate the proposed design methodology, a second 40-cell multiplexer layout was designed using similar polarization-interaction perception and clocking strategy. *Figure 6* displays the simulation waveform of 40-cell design that correspondingly shows correct input selection and output generation for all select line combinations.

Table 4. Performance Analysis for proposed QCA-based Multiplexer Design

DESIGN/Year	CELLS	AREA (μm^2)	LATENCY (clock cycles)
T. Purkayastha [7]/2018	110	0.16	1.25
N. Patahak [16]/2019	177	0.24	0.25
L.Xingjun [8]/2019	92	0.12	1.25
M.Mosleh [9]/2020	82	0.10	1.5
S. Banerjee [17]/2020	67	0.08	2.5
H. Rashidi [18]/2021	96	0.11	1
J.C. Jeon [10]/2021	79	0.10	1.5
T. Bagheri [15]/2024	50	0.08	1
Jana [19]/2025	37	0.012	5
M. Zohaib [16]/2025	105	0.15	2.5
Proposed design.1	45	0.06	1
Proposed design.2	40	0.07	1

Table 4 shows comparative performance analysis with the proposed designs. By considering data shown above it clearly shows the enhancement of proposed design in terms of structural complexity and area utilization in contrast with prevailing architectures. Although some recent designs exhibit lower cell count or area but the proposed multiplexer maintains a latency of 1 Clock Cycle and also shown improvement in energy efficiency as shown in *table 9*. The results shows that the given design deliver an effective trade-off among compactness and computational speed.

5. ENERGY DISSIPATION ANALYSIS FOR PROPOSED DESIGN USING QCA DESIGNER-E

With the aim of analyse the power metrics of anticipated mux design we used QCA Designer-E which offers decidedly precise context by trailing dynamic quantum states of individual cell across circuit layout. QCA Designer-E statistically participating the Liouville Equation and estimates the real time non-adiabatic energy losses into the environment throughout clock transitions. Appraisal of energy dissipation by QCA Designer is castoff as its expressions how precisely layout compacting, clock-zone routing and electrostatic cell interactions impression thermal performance. The comprehensive data investigation for proposed design by consuming QCA Designer-E delivers the initial proof desirable to validate the structural optimizations and substantiation of the design. In QCA Designer-E energy dissipation analysis executed by modelling each QCA cell as a two-state quantum system. QCA Designer-E offers two methods for energy estimation one is Euler's method and second is Runge- Kutta method and accordingly delivers results contingent upon by what means vector state relaxation and external clock switching interrelate. In QCA Designer-E performance of energy dissipation analysis is done by selection of Coherence Energy vector simulation engine that utilizes Coherence vector and Hamiltonian vector. The time progression of cell's state including environmental degeneracy is completed by Quantum Liouville Equation (Lindblad Master Equation) given as:

$$\frac{d\vec{\lambda}}{dt} = \frac{2}{h}(\vec{\Gamma} \times \vec{\lambda}) - \vec{R}$$

Where:

$\vec{\Gamma} \times \vec{\lambda}$ = Coherent, non-dissipative rotation of the state

$\vec{R}$=Relaxation vector tracking energy dissipation to the environment given by

$$\vec{R} = \frac{1}{\tau}\,[\vec{\lambda} - \overrightarrow{\lambda_0}\,]$$

Here, $\boldsymbol{\tau}$ =Relaxation time and $\overrightarrow{\lambda_0}$ is the instantaneous thermal equilibrium vector.

There are two numerical solvers available under Coherence - Energy Vector simulation engine in QCA Designer-E and we performed both methods to confirm the thermal stability of our proposed design and the two available numerical solvers are:

1. Euler's Method
2. Runge-Kutta Method

Euler's Method is well-thought-out as first-order numerical method. It projects the next state linearly along the current derivative slope over a minute step Δt and is given by equation:

$$\vec{\lambda}(t + \Delta t) = \vec{\lambda}(t) + \Delta t.[\frac{2}{h}\left(\vec{\Gamma}(\boldsymbol{t}) \times \vec{\lambda}(t)\right) - \frac{1}{\tau}$$

Second method is Runge-Kutta method which is a 4^{th} order method which trials the derivative at four diverse points across interval Δt in directive to hypothesis an extremely accurate average slope. Now the four trial slopes in RK4 Method are (k1, k2, k3, k4):

$$k1 = f(t_n, \overrightarrow{\lambda_n})$$

$$k2 = f\left(t_n + \frac{\Delta t}{2}, \overrightarrow{\lambda_n} + \frac{\Delta t}{2}k1\right)$$

$$k3 = f(t_n + \frac{\Delta t}{2}, \overrightarrow{\lambda_n} + \frac{\Delta t}{2}k2)$$

$$k4 = f(t_n + \Delta t, \overrightarrow{\lambda_n} + \Delta t k3)$$

The main equation thus becomes:

$$\overrightarrow{\lambda_{n+1}} = \overrightarrow{\lambda_n} + \frac{\Delta t}{6}(k1 + k2 + k3 + k4)$$

For proposed design in order to find energy dissipation by Euler's method/Runge-Kutta Method we need to select Coherence-Energy vector simulation engine with the specifications as shown in *table 5* where we select Euler's

Method/Runge-Kutta Method in the selection option out of two methods and perform the simulation. *Table 6* shows the complete energy dissipation analysis values for both methods. By default, in QCA Designer E it gives results in Euler's Method under Coherence-vector Energy simulation setup engine.

Table 5. Specifications for QCA designer E for energy dissipation analysis by Euler's Method/Runge-Kutta Method

QCA Designer -E design setup for Euler's Method/ Runge-Kutta Method (Coherence Vector Energy)		
Specification	**Value**	**Unit**
Temperature	1.000000	K
Relaxation Time	1.000000e-015	s
Clock Period	4.000000e-012	s
Input Period	4.000000e-012	s
Time Step	1.000000e-016	s
Total Simulation Time	5.000000e-011	s
Clock High	9.800000e-022	J
Clock Low	3.800000e-023	J
Clock Shift	0.000000e+000	
Clock Slope (RAMP, GAUSS)	1.000000e-012	s
Radius of Effect	80.000000	nm
Relative Permittivity	12.900000	
Layer Separation	11.500000	nm

Table 6. Energy Dissipation Analysis of designed 4:1 MUX using QCA Designer-E for Euler's Method and Runge -Kutta Method

Euler's Method Energy Dissipation Analysis			Runge-Kutta Energy dissipation Analysis		
E_bath_total	**E_clk_total**	**E_Error_total**	**E_bath_total**	**E_clk_total**	**E_Error_total**
1.6230e-003	1.0024e-003	-1.5747e-004	1.7412e-003	9.7659e-004	-6.7167e-005
7.4935e-004	2.8968e-003	-5.8584e-005	8.1377e-004	2.8736e-003	-1.7389e-005
1.5914e-003	2.1995e-003	-1.5375e-004	1.7068e-003	2.1748e-003	-6.5169e-005
1.5888e-003	2.0954e-003	-1.5189e-004	1.7003e-003	2.0729e-003	-6.3267e-005
2.2009e-003	2.0037e-004	-2.2189e-004	2.3516e-003	1.7490e-004	-9.8944e-005
1.3272e-003	2.0948e-003	-1.2301e-004	1.4242e-003	2.0719e-003	4.9166e-005
2.1693e-003	1.3975e-003	-2.1817e-004	2.3172e-003	1.3731e-003	-9.6949e-005
9.2452e-004	2.9824e-003	-7.8346e-005	9.9873e-004	2.9596e-003	-2.7252e-005
9.6356e-004	1.7761e-003	-8.2609e-005	1.0414e-003	1.7517e-003	-2.9388e-005
1.4244e-003	2.1056e-003	-1.3478e-004	1.5304e-003	2.0807e-003	-5.5645e-005
1.6787e-003	2.1140e-003	-1.6336e-004	1.7988e-003	2.0894e-003	-6.9855e-005
Total energy dissipation (Sum_Ebath): 1.62e-002 (Error: ± -1.54e-003 eV)			Total energy dissipation (Sum_Ebath): 1.74e-002 eV (Error: ± -6.40e-004 eV)		
Average energy dissipation per cycle (Avg_Ebath): 1.48e-003 eV (Error: ± -1.40e-004 eV)			Average energy dissipation per cycle (Avg_Ebath): 1.58e-003 eV (Error: ± -5.82e-005 eV)		

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Table 6 displays the energy dissipation outline of the premeditated multiplexer (MUX)by means of both Euler's Method and Runge-Kutta method so as to appraise its ultra-low-power performance within the Quantum Dot Cellular Automata domain. Operative entirely outside the standard of conventional I2R ohmic losses, the premeditated MUX layout confirmation minimization of energy dissipation by augmenting cell placement and confirming adiabatic state transitions all through clocking phases. Mathematical depiction by means of Euler's method confirmations a total energy dissipation of 1.62×10^{-2} eV with an average dissipation per clock cycle of 1.48×10^{-3} eV by an error margin of ± -1.40×10^{-4} eV. For corresponding corroboration Runge-Kutta method delivers a more detailed trailing of quantum states and displays total energy dissipation of 1.74×10^{-2} eV and an average cycle dissipation of 1.58×10^{-3} eV with an error margin of ± -5.82×10^{-5} eV. These standards confirm that the designed MUX architecture efficaciously restrictions heat transfer to the neighbouring environment (E_bath_total) and thus reduces the dynamic clocking overhead (E_clk_total) and founding its feasibility as exceedingly energy efficient design primitive for next generation nano electronic circuits.

The energy dissipation analysis as shown in *figure 7* highlights the superior thermodynamic efficiency of the proposed MUX design. Under baseline operations, the average energy dissipated per clock cycle endure constrained to ultra-low value of 1.48×10^{-3} eV with Euler's method and 1.58×10^{-3} eV with Runge-Kutta method. The constricted convergence amid first-order Euler's calculation and higher-order Runge-Kutta method mathematically corroborates the operational integrity of the design and consequently corroborative that the premeditated layout successfully suppresses erratic non-adiabatic switching losses and structural leakage paths.

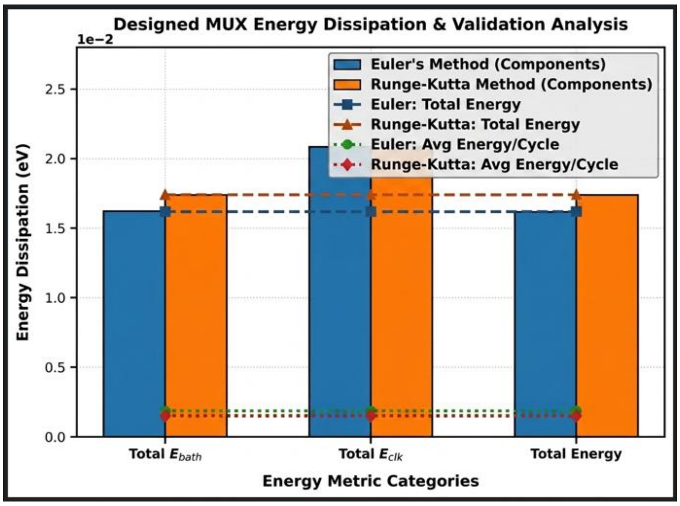

Figure 7. Energy Dissipation using Euler's Method and Runge-Kutta Method for Proposed Multiplexer Design

In order to corroborate the thermal stability of the specified design we premeditated the energy dissipation values by varying the temperature from 1K to 1K for both the procedures castoff for estimation which are Euler's Method and Runge -Kutta Method. *Table 7* demonstrations comprehensive energy dissipation analysis of designed MUX with temperature variations and recorded data validates exceptional thermal stability and consequently sustaining a decidedly outstanding energy consequence. By considering the statistics from higher-order Runge-Kutta analysis the total energy dissipation upsurges only marginally from1.74×10^{-2} eV at 1K to 1.78×10^{-2} eV at 5K. Likewise the data from Euler's method demonstrations that steady inclination is emulated with average energy restricted between 1.48×10^{-2} eV and 1.51×10^{-2} eV with variation in Temperature from 1K to 5K. Hence, both mathematical representations substantiate that the design functions consistently within the ultra-low energy province and providing the robust adiabatic switching proficiencies of the augmented MUX architecture even with disparity of temperature.

Table 7. Euler's Method for proposed MUX for Energy Dissipation with Temperature variation

Euler's Method with Temperature Variation				
Tempera-ture (T) K	**Total energy dissipation (Sum_Ebath) (eV)**	**Error (eV)**	**Average energy dissipation per cycle (Avg_Ebath) (eV)**	**Error(eV)**
1K	1.62e-002	± -1.54e-003	1.48e-003	± -1.40e-004
2K	1.62e-002	± -1.54e-003	1.48e-003	± -1.40e-004
3K	1.63e-002	± -1.54e-003	1.48e-003	± -1.40e-004
4K	1.64e-002	± -1.55e-003	1.49e-003	± -1.41e-004
5K	1.66e-002	± -1.57e-003	1.51e-003	± -1.43e-004

Table 8. Runge Kutta Method for Proposed MUX for Energy Dissipation with Temperature variation

Runge-Kutta Method with Temperature Variation				
Tempera-Ture (T) K	**Total energy dissipation (Sum_Ebath) (eV)**	**Error**	**Average energy dissipation per cycle (Avg_Ebath) (eV)**	**Error**
1K	1.74e-002	± -6.40e-004	1.58e-003	± -5.82e-005
2K	1.74e-002	± -6.39e-004	1.58e-003	±- -5.81e-005
3K	1.74e-002	±- -6.37e-004	1.59e-003	± -5.79e-005
4K	1.76e-002	± -6.40e-004	1.60e-003	± -5.82e-005
5K	1.78e-002	± -6.48e-004	1.62e-003	± -5.89e-005

Figure 8 shows the estimation investigation of thermodynamic reliability of the anticipated MUX design at diverse temperature disparity from 1K to 5K. The near-linear graphs confirmations least deviation of both Total Energy dissipation

and Average Energy dissipation and consequently confirm robust thermal stability of the designed MUX. These confirmations that the premeditated MUX layout supresses thermal-noise persuaded polarization affronts and consequently sustaining a rigid potential barrier.

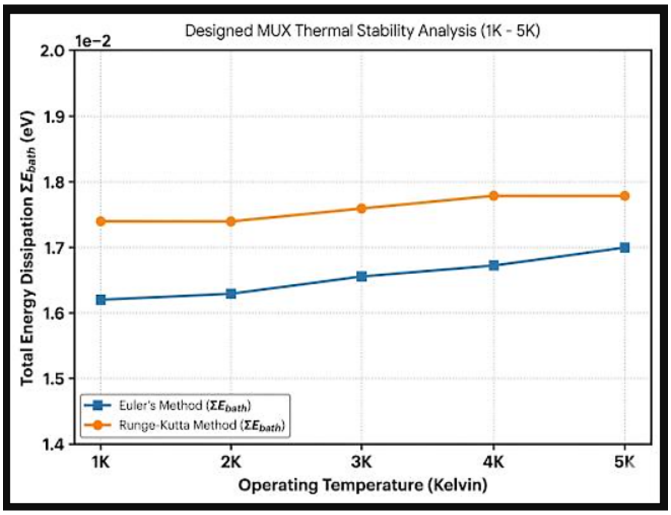

Figure 8. Thermal stability Investigation of proposed MUX using Euler's Method and Runge-Kutta Method

Table 9 displays comparison analysis of proposed Mux design in terms of energy dissipation compared to several state-of -art designs from recent literature. The statistics in *table 9* confirmations that the anticipated design attains lowest energy footprint across both appraised metrics. The comparative data clearly demonstrates that the proposed 2026 design achieves the lowest energy footprint across both evaluated metrics. This substantial saving in energy metrics for proposed design corroborates that the specified design curtails the thermal-noise persuaded polarization outrages though sustaining a rigid potential barrier and make the premeditated architecture apposite for ultra-low-power applications.

Table 9. Energy Dissipation Comparative Analysis or Proposed 4:1 MUX

Design/ Year	Total Energy Dissipation (meV)	Average Energy Dissipation (meV)
Bahar [20]/2020	97.1	15.65
Majeed [21]/2020	27.73	4.76
Alkaldy [22]/2020	19.42	2.54
Rezai [23]/2018	17.9	1.63
Jana [19]/2025	-	2.47
Proposed /2026	16.2	1.48

As shown in *figure 9* in assessment with existing architectures, the anticipated MUX accomplishes an energy efficiency upgrading of up to 83.32% in total energy dissipation and 90.54% in average energy dissipation.

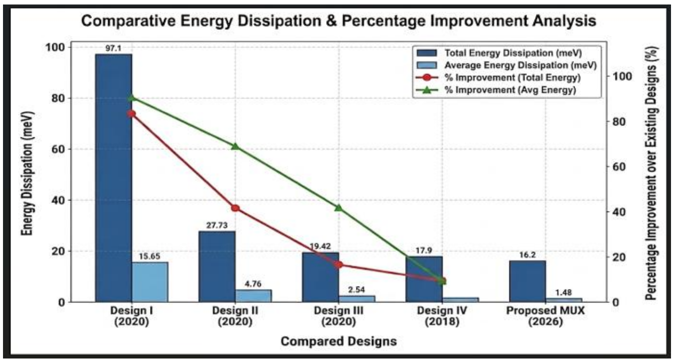

Figure 9. Comparative Analysis of Proposed MUX for energy dissipation

6. FAULT TOLERANCE ANALYSIS

As the information in QCA-based designs propagated on the basis of localised quantum mechanics of cell-to-cell electrostatic coupling unlike CMOS designs where logic values are dictated by continuous voltage level, therefore, it is necessary to evaluate structural defects so as to ensure if a nanoscale design can survive real-world chemical synthesis or lithographic fabrication. The fundamental unit of data processing in QCA-based designs is the cell-polarisation, which directions the charge distribution of electrons within quantum dots. By taking into consideration ideal conditions, a driving cell forces neighbouring cell into a corresponding polarization state so as to sustain the lowest energy configuration. However, during fabrication nonconformity from the ideal grid layout can transpire. The stability of the entire circuit thus depends upon how these geometric variations vary the localised Kink energy (Ek). The Kink energy thus represent the electrostatic energy associated with mismatched neighbour polarization contrasted with a correct state that is matching neighbour polarizations [25]. The mathematical equation that shows this interaction in between two adjacent cells, cell '*i*' and cell '*j*' is expressed as:

$$E_k = \frac{1}{4\pi\varepsilon_o\varepsilon_r}\sum_{m=1}^{4}\sum_{n=1}^{4}\frac{q_m q_n}{|r_{i,m} - r_{j,n}|}$$

Where,
ε_o=Permittivity of vacuum
ε_r=Relative permittivity of the underlying substrate
$q_m q_n$=Localised charges of internal dots
$|r_{i,m} - r_{j,n}|$=Strict physical distance vector separating the quantum dots

By following the foundational defect classification frameworks established in literature there are primarily three structural fault conditions that disturb the layout reliability:

1. **Missing Cell Defects (Deletion/Omission)**

This type of defect transpires when a synthesis failure origin a comprehensive drop-out of a cell on the grid. This acquaint with an unanticipated spatial gap that can be tested to check if remaining Coulombic field can still bridge the distance.

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2.Extra Cell Defects (Deposition/Additional)
This type of defects transpires when stray, unsolicited cell settles in a position adjacent to the active layer region. This injects parasitic crosstalk and develop unsolicited electrostatic behaviour into the system.

3.Cell Misalignment Defects (Displacement/The Nudge)
These types of defects occur when a cell remains functional but is physically shifted along the horizontal (ΔX) or vertical (ΔY) axis by a few nanometres [24].

As Fault tolerance is an significant performance metric in QCA-based designs due to possibility of fabrication-induced defects, therefore, in this work cell omission and cell misalignment analysis were performed depending upon the cell layout design of proposed Multiplexer for design.1.The subsequent output waveforms were compared with the Fault-free response so as to determine the effect of each defect on circuit functionality and to evaluate the overall robustness of the design .

Figure 10 shows the annotated layout of proposed QCA Multiplexer with cells labelling that are used during cell omission analysis. In order to examine the effect of fabrication defects, the illustrative cells were selected from three functional regions of the designed layout *i.e.* Region.1, Region.2 and Region.3 which are acting as signal propagation region, interaction region or decision-making region and the output region. The omission of these cells was exclusively inspected through simulation and the subsequent output waveforms were associated with the fault-free design. This region-based selection qualifies the identification of critical and non-critical cells while providing insight into the robustness of the designed layout against manufacturing-induced defects.

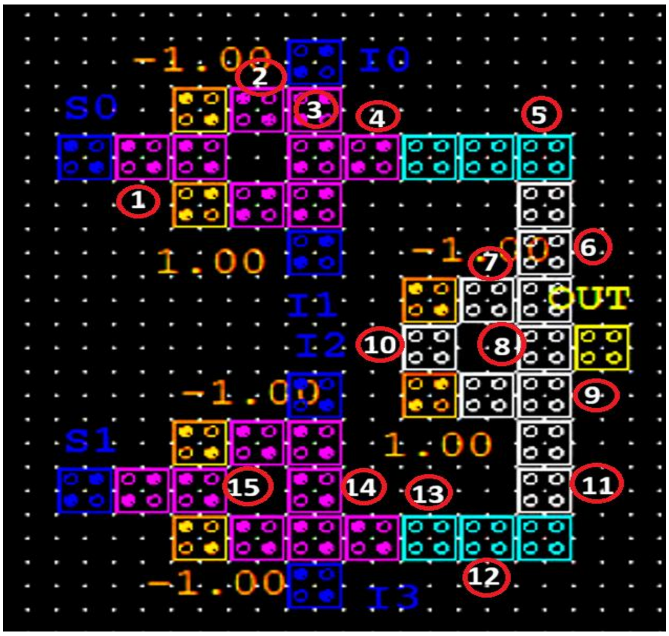

Figure 10. Unique cell selection for Cell-Omission Fault Analysis

With the intention of measure, the structural flexibility of proposed design we executed a confined single cell omission fault analysis. A sample population of 15 unique cells labelled C_1 to C_{15} as shown in figure was steadily analysed under imperfection conditions so as to perceive their direct influence on terminal logic state. As shown in *table 10* the proposed design shows the inherent structural redundancy where out of 15 simulated cell nodes, 10 cells were classified as completely tolerant so their individual failure or severe degradation does not affect the functional output of logic state. However, the remaining 5 cells were identified as Faulty as they change the waveform if get omitted or get defected.

Table 10. Cell Omission Fault Analysis for Proposed MUX Design

Cell Number	Behaviour	Cell Number	Behaviour
C_1	MUX	C_9	FAULTY
C_2	MUX	C_{10}	MUX
C_3	MUX	C_{11}	MUX
C_4	MUX	C_{12}	MUX
C_5	FAULTY	C_{13}	MUX
C_6	FAULTY	C_{14}	MUX
C_7	FAULTY	C_{15}	MUX
C_8	FAULTY	-	-

Total Number of Cells taken for Analysis=15

Total Number of Tolerant Cells=10

Total Number of Faulty Cells=5

$$\text{Fault Tolerance (\%)} = \left(\frac{Number\ of\ Tolerant\ cells}{Total\ Number\ of\ Unique\ cells\ Tested} \times 100\right)$$

$$\text{Fault Tolerance} = \left(\frac{10}{15}\right) \times 100 = 66.67\%$$

The overall fault tolerance percentage of 66.67% shows that the given design yields a robust structural fault tolerance. Therefore, the proposed Multiplexer sustains high structural integrity and consistent signal propagation even when exposed to significant localized manufacturing imperfections.

In order to compliment the cell omission fault analysis shown, a comprehensive physical displacement analysis also executed so as to estimate the designed layout stability against lithographic misalignment defects. Cell misalignment or displacement defect is common fabrication defect in QCA-based designs where a cell diverges from its position. The deviation in cell position amends the electrostatic interaction between neighbouring cells and can disturb polarization propagation. In order to evaluate the robustness of proposed Multiplexer design, representative cells shown in *figure 11* from different interaction regions were exposed to controlled positional displacement of 5nm,10nm and 15 nm. The resultant output response is classified as Valid, Degraded or Faulty in comparison with fault-free waveform.

Table 11. Cell Displacement Fault Analysis for proposed MUX design

Cell	Displacement/Misalignment		
	5nm	10nm	15nm
C_1	Valid	Valid	Valid
C_4	Valid	Degraded	Degraded
C_5	Valid	Valid	Faulty
C_7	Faulty	Faulty	Faulty
C_{10}	Valid	Valid	Valid
C_{11}	Valid	Degraded	Valid
C_{14}	Valid	Faulty	Faulty
C_{15}	Valid	Degraded	Valid

By considering the results of *table 10* we can calculate the Functional Survival Rate (FSR) of the designed layout by considering Valid, Degraded states as:

$$FSR(\%) = \frac{N_V + N_D}{N_T} \times 100$$

Where:

N_V=Number of Valid cases

N_D=Number of degraded cases

N_T=Total number of tested cells

By using above equation for 5nm,10nm and 15nm displacement we get:

$$FSR_{5nm} = \frac{7}{8} \times 100 = 87.50\%$$

$$FSR_{10nm} = \frac{7}{8} \times 100 = 87.50\%$$

$$FSR_{15nm} = \frac{7}{8} \times 100 = 75.00\%$$

The misalignment fault analysis results as shown in *table 11* shows that the proposed layout design is stable towards variation with different displacement values. At 5nm displacement seven out of eight cells sustained correct functionality resulting in FSR of 87.5%. On increasing displacement to 10nm there is performance degradation in several cells, however, functionality remain conserved in seven out of eight cases, sustain an FSR of 87.5%. with displacement value of 15nm larger number of cells experienced failure or degradation which reduces the FSR to 75%. Therefore it validates that the proposed architecture has sustainability towards restrained fabrication-induced positional discrepancies while preserve the reliable logic operation.

The misalignment results show same trend as that of cell omission analysis. Cells located in a strongly coupled interaction region persist functional even under larger positional displacement although cell belongs to weaker coupling regions show degraded or faulty behaviour. This observation is also consistent with Kink energy analysis where regions with higher Kink energy establish stronger electrostatic coupling and improved fault tolerance. Consequently, the fault analysis confirms that the robustness of proposed multiplexer directly associated to the interaction strength between neighbouring QCA cells.

7. KINK ENERGY ANALYSIS

In order to estimate the thermodynamic stability and robustness of the designed architecture contrary to thermal dissention and digital polarization error, Kink energy analysis performed in this section. The Kink Energy is defined as the energy difference between two adjacent QCA cells when they are in an identical that is Matched polarization versus when they are in opposite that is Mismatched or Kinked polarization state. Mathematically, a higher the Kink energy value is stronger is the electrostatic coupling between neighbouring cells which confirm that the logic state propagates consistently deprived of fluctuating due to thermal noise [22]. In complex layout designs, cells experience different geometric configurations depending upon the architectural placement, therefore, the proposed design is segmented into four primary localized interaction regions so as to estimate structural integrity that includes: standard straight wires, Corners/bends, Majority gates and coupling boundaries. The fundamental electrostatic energy V_{AB} in between two interacting cells A and *B* is specified by Coulomb's Law which sum the interactions between all internal charge centres and is given as:

$$V_{AB} = \frac{1}{4\pi\varepsilon_0\varepsilon_r} \sum_{i=1}^{4} \sum_{j=1}^{4} \frac{q_i^A q_j^B}{\left| r_i^A - r_j^B \right|}$$

Where, $q_i^A q_j^B$ represent the localized quantum dot charges. ε_0 is the vacuum permittivity (8.854×10^{-12} F/m) and ε_r is the relative permittivity of the material substrate (for standard GaAs/AlGaAs=12.9).

The Kink energy between cell A and B is defined as the difference in energy between there opposite polarization state and their identical polarization state:

$$Ek = \sum_{i=1}^{4} \sum_{j=1}^{4} \frac{q_i q_j}{4\pi\varepsilon_0\varepsilon_r} \left(\frac{1}{r_{ij}^{mismatched}} - \frac{1}{r_{ij}^{matched}}\right)$$

By considering designed layout for Multiplexer, we assume r1 and r2 as: r1 is the minimum distance that is centre-to-centre distance from the target cell to the closest interacting cell in that region and r2 is the maximum distance that is centre-to-centre distance to the furthest interacting cell within that specific localized sub-circuit structure as shown in *figure 11*.

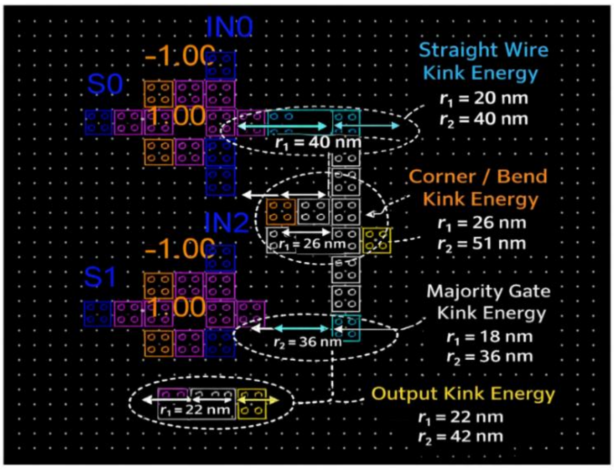

Figure 11. Interaction Region Selection for Kink Energy Calculation

The Kink Energy value depending upon the effective distance approximation formula by using distance r1 and r2 where r1 is nearest interacting boundary and r2 is the farthest interacting boundary of that region it is given as:

$$Ek = \frac{e^2}{4\pi\varepsilon_0\varepsilon_r} . (\frac{1}{r1} - \frac{1}{r2})$$

Here, $\frac{e^2}{4\pi\varepsilon_0\varepsilon_r} \approx 1.115 \times 10^{-10} eV.m = 0.1115 eV$

Table 12. Kink Energy Analysis for Proposed MUX Design

Interaction region	r1(nm)	r2(nm)	Kink Energy(eV)
Straight wire	20	40	2.77×10^{-3}
Corner/Bend	26	51	1.89×10^{-3}
Majority gate	18	36	3.10×10^{-3}
Output coupling	22	42	2.31×10^{-3}

From above analysis as it is concluded that the designed layout exhibits robust thermodynamic stability. From *table 12* it is clear that Majority Gate where logic decisions are finalised, accomplishes highest polarization energy recorded as3.10×10^{-3} eV which ensuring strong intercell coupling. The corner region conquers a stable energy barrier with value 1.89×10^{-3} eV in spite of the geometric displacement. This shows that the stability of the proposed design.

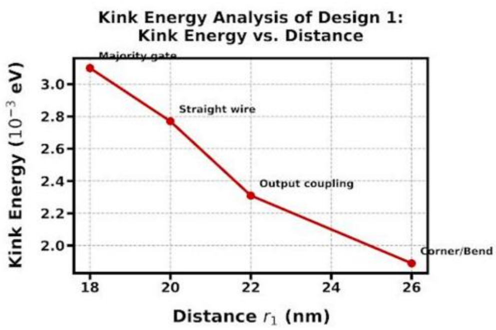

Figure 12. Kink Energy Analysis for Proposed Design

By correlating Kink energy as discussed depending upon main interaction regions and correlating the Fault Analysis results discussed above, we conclude the following analysis;

Table 13. Correlation of Kink Energy and Cell Omission Fault Tolerance for Proposed MUX Design

Interaction Region	Kink Energy (eV)	Cells	Omission Results
Straight wire	2.77×10^{-3}	C4, C5	Functional/Degraded
Corner	1.89×10^{-3}	C7, C8, C9	Degraded
Majority Gate	3.10×10^{-3}	C12, C13, C14	Functional
Output Region	2.31×10^{-3}	C8, C9, C10, C12	Functional/Degraded

The fault analysis results and Kink Energy analysis shows a clear relationship in order to show circuit robustness. Regions possessing high value of Kink Energy exhibits stronger polarization coupling and therefore maintain reliable signal propagation even if cells were omitted. In contrast, regions with lower Kink energy value are more vulnerable to defects because of weaker intercellular interactions which reduces the ability of neighbouring cells to preserve the intended polarization state. The Majority gate Interaction region shows higher Kink Energy of 3.10×10^{-3} eV which specifies the strong coupling and cells omission fault analysis for that area confirmation Functional Behavior as shown in *table 13*. Corner/bend region displays minimum Kink energy and the fault cell omission fault analysis under that area confirmations degraded function. Other two area that is Straight wire and Output region demonstrations less energy than Majority Gate region and more energy than Corner bend region so cell omission fault analysis for that regions display Functional/Degraded behavior where some cell omission displays Functional behavior and other Degraded.

8. POLARIZATION ENERGY ANALYSIS

In Qunatum Dot Cellular Automata based designs the thermodynamic stability and logic state stability of the layout can be appraised by two energy metrics: Kink Energy and polarization energy. Kink energy (Ek) is defined as the fundamental electrostatic energy difference that transpires when two adjacent cells are driven into opposite polarization states like if +1 state cell interacting with -1 state cell. Thus, this signifies the confined thermodynamic barrier of the cell configuration in contradiction of unwanted logic transitions or errors caused by external noise. While Kink energy evaluates the localized coupling between two cells, Polarization energy (Etotal) measures the system-level aggregate of these electrostatic interactions across the overall layout of QCA based designs. In QCA based designs this total energy computes the cumulative effect of mutually interacting fields along X-direction and Y-direction and therefore acts as important standard for overall circuit stability and signal propagation reliability. For anticipated Multiplexer design polarization energy analysis was executed by considering the interaction cells from X-direction and Y-direction as shown in

Figure.13 in order to evaluate the stability of cell interactions. The discrete interaction energy components i.e. Eix and Eiy of the proposed layout design are mathematically assessed using electrostatic power-law drop-off model established within QCA Designer Bistable simulation engine framework. For standard specifications in QCA Designer bistable simulation engine QCA cells size dimensions are well-thought-out as 18nm×18nm and a minimal center-to-center displacement distance is considered as 20nm and baseline electrostatic kink energy is defined as 11.9 meV. The physical interaction energy among target cell and its neighboring cells along X-axis and Y-axis reduces as a function of distance conferring to standard quadrupole interaction relationship:

$$E_i = E_k \left(\frac{r_{baseline}}{r_i}\right)^5$$

Where:

r_i denotes the specific co-ordinate distance form X-direction or Y-direction (r_{ix} or r_{iy}) of the interacting cell.
$r_{baseline}$=20nm (The standard minimum cell spacing)

In order to determine the aggregate polarization dynamics of the multiplexer architecture, the discrete directional energy parameters are linearly accumulated across the system layout.

The cumulative polarization energies for X-direction and Y-direction are calculated as:

$$E_X = \sum_{i=1}^{n} E_{iX}$$

$$E_Y = \sum_{i=1}^{n} E_{iY}$$

Consequently, the total polarization energy (E_{TOTAL}) can be calculated as:

$$E_{TOTAL=}E_X + E_Y$$

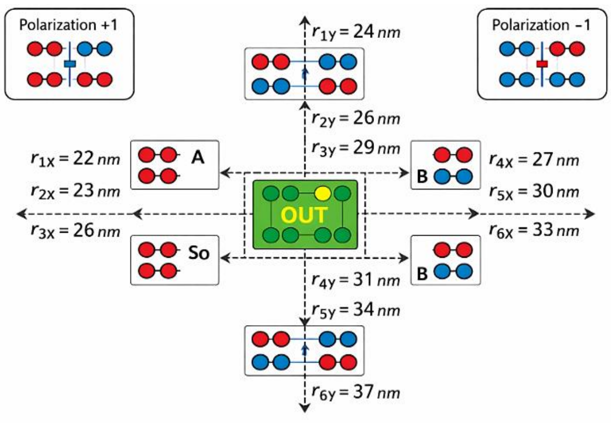

Figure 13. Cell Displacement Diagram for proposed Design

By substituting the values of distances from X-direction and Y-direction to the given equations we can find out the Polarization energy of the designed layout as given in *table 15,16.*

Table 15. Polarization Energy Analysis of Proposed MUX Design in X-Direction

X-direction interaction	r_{IX}(nm)	Energy Eix(meV)	Energy E_{Ix}(J)
E_{1X}	22	8.41	1.347×10^{-21}
E_{2X}	23	7.96	1.275×10^{-21}
E_{3X}	26	6.88	1.102×10^{-21}
E_{4X}	27	6.52	1.044×10^{-21}
E_{5X}	30	5.94	0.951×10^{-21}
E_{6X}	33	5.31	0.850×10^{-21}

Table 16. Polarization Energy Analysis of Proposed MUX Design in Y-Direction

Y-direction interaction	r_{IY} (nm)	Energy (meV)	Energy E_{IY}(J)
E_{1Y}	24	7.85	1.257×10^{-21}
E_{2Y}	26	7.12	1.140×10^{-21}
E_{3Y}	29	6.47	1.036×10^{-21}
E_{4Y}	31	6.01	0.962×10^{-21}
E_{5Y}	34	5.44	0.871×10^{-21}
E_{6Y}	37	4.98	0.797×10^{-21}

Therefore, we get

$$E_X = \sum_{i=1}^{n} E_{iX} = 41.02 \text{ meV} = 6.571\times10^{-21} \text{ J}$$

$$E_Y = \sum_{i=1}^{n} E_{iY} = 37.87 \text{meV} = 6.066\times10^{-21} \text{ J}$$

$$E_{TOTAL=}E_X + E_Y = 78.89 \text{ meV} = 1.263\times10^{-21} \text{ J}$$

In QCA-based designs a larger aggregate polarization energy (E_{TOTAL}) is highly necessary as it specifies robustness and stability of the design. From thermodynamic perspective, higher polarization energy is essential for stable logic states operation and also consequences in upsurge of localized energy barrier which avoids any instability in the logical correctness caused by environmental noise or parasitic signal cross-talk. Therefore, the polarization analysis performed for 4:1 Multiplexer design so as to verify structural reliability of the designed layout. Based on the distance-dependent electrostatic drop-off model, the individual cell interaction metrics along the orthogonal co-ordinate axes recorded total X-direction polarization energy (E_X) of 41.02 meV and total Y-direction polarization energy (E_Y) of 37.87 meV. Therefore, the overall circuit layout achieves a Total polarization energy (E_{TOTAL}) as 78.89 meV.

9. PRACTICAL FABRICATION CHALLENGES AND IMPLEMENTATION CONSIDERATIONS

Even though the proposed QCA -based Multiplexer design establishes correct logical functionality, low energy dissipation and Fault tolerance characteristics as conferred above but there are several practical challenges persist for physical implementation. First challenge is fabrication accuracy which is a critical issue in QCA-based designs because due to insignificant cell displacement, omission, or misalignment there should be discrepancy ensue between electrostatic interaction between neighbouring cells. To investigate this aspect, cell omission and misalignment analysis were executed in the anticipated work which shows that the proposed architecture sustains functional operation under restrained manufacturing imperfections. Second main challenge is Thermal noise which affect the reliability of the QCA-based designs. As temperature increases, thermal fluctuations may disturb cell polarization states and therefore, reduces the stability of the information propagation. This demand sustaining adequate intercellular coupling strength which is essential for reliable operation of the design. The Kink energy analysis accomplished in this work shows that the designated interaction regions possess adequate coupling strength so as to sustenance the stable polarization transfer. Clock synchronization is another challenge which plays a significant role in QCA -based implementations. Subsequently information propagation depends on the four-phased clocking in QCA -based layouts, indecorous clock zone assignment can acquaint with signal delay and polarization degradation. In the proposed layout design, clock zones were carefully allocated so as to ensure synchronized data propagation and stable output generation. Moreover, large scale QCA -integration remain challenging because of fabrication intricacy and process variability. Future work may investigate advance fabrication techniques, multilayer architectures, and improved clocking schemes so as to further enhances robustness and manufacturability. The attained fault tolerance and kink energy results confirmed that the proposed multiplexer possesses capable characteristics for reliable nanoscale QCA-based implementations.

10. CONCLUSIONS

This work demonstration the design and simulation of QCA-based 4:1 Multiplexer design using region-based design approach. The anticipated design was functionally substantiated by using QCA Designer 2.0.3 and estimated in terms of structural complexity, energy dissipation and fault tolerance characteristics. Energy analysis was executed using QCA Designer-E tool by employing both Euler's method and Runge-Kutta Method. The attained outcomes confirmed low energy ingesting though sustaining correct logic functionality. To further examine the designed architecture robustness, cell omission and cell displacement fault tolerance analysis were conducted. The cell omission fault tolerance analysis exhibited functional survival rates of 66.67%, whereas the misalignment analysis exposed functional persistence rates of 87.5%,87.5% and 75% for displacement values of 5nm,10nm and 15 nm. Moreover, the correlation amid kink energy and fault tolerance revealed that regions with stronger intercellular coupling unveiling improved resistance to fabrication-induced defects. Based on the simulation results, the proposed Multiplexer demonstrations satisfactory functional performance, energy characteristics, and robustness within QCA Simulation environment. The obtainable analyses deliver valuable perception into the behaviour of region-based QCA-based Multiplexer structures and can serve as a reference for future simulation-oriented surveys of QCA logic designs.

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