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Analytical Method for Evaluating HD3 in CMOS LC Oscillators

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ABSTRACT- This paper presents an analytical method for evaluating the third harmonic distortion (HD3) of the CMOS LC oscillator employing cross-coupled MOS differential pair. By assuming that the current generated by the cross-coupled differential pair and flowing through the LC tank is a square wave, a closed-form solution for HD3 is derived. To validate the theoretical analysis, simulations were performed, showing good agreement between the predicted and simulated results.

Keywords: Oscillator, Harmonic Distortion, Circuit Analysis, Nonlinear Distortion, Analog Integrated Circuits.

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1. INTRODUCTION

A high-quality oscillator is a fundamental building block in modern communication systems.

Ideally, it should generate a perfectly sinusoidal waveform with high spectral purity to ensure reliable system performance. Among the key performance metrics, phase noise has received significant attention because it directly affects the frequency stability and spectral characteristics of oscillators, particularly in wireless communication systems [1–3]. In practical implementations, however, nonlinear device characteristics introduce harmonic distortion, which degrades signal purity and contributes to spectral degradation. Therefore, understanding and predicting harmonic distortion is essential for improving oscillator performance. Evaluation of the harmonic content of electronic oscillators is thus important, and a number of mathematical techniques for analyzing nonlinear oscillations have been developed [4–7].

Previous studies have analyzed harmonic distortion in Wien-type oscillators [5], Colpitts oscillators [6], and MOS RLC oscillators [7]. To the best of the authors' knowledge, no harmonic distortion analysis has been reported for the LC oscillator proposed in this work. In this paper, a closed-form expression for the third harmonic distortion (HD_3) is derived by directly evaluating the ratio of the fundamental component to the third harmonic component, leading to a simple and intuitive analytical approach. The third harmonic distortion (HD_3) is the main harmonic distortion, of CMOS LC oscillators employing cross-coupled MOS differential pair is derived. The derivation is based on the assumption that the current produced by the cross-coupled pair flowing through the LC tank is a square wave, which causes differential voltage of the oscillator to contain harmonic components.

2. EQUIVALENT CIRCUITS OF CMOS LC OSCILLATORS

The widely used LC CMOS oscillator, which consists of an LC tank and a cross-coupled MOS cross-coupled pair, is shown in *fig. 1* and its differential output voltage can be expressed as

$$V_D(t) = V_1 \sin(\omega_0 t) + V_3 \sin(3\omega_0 t) + \cdots \quad (1)$$

Where

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (2)$$

and V_1 and V_3 are the fundamental and third harmonic components respectively.

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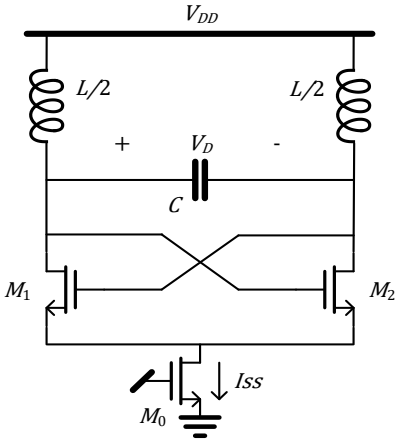

Figure 1. CMOS LC oscillators

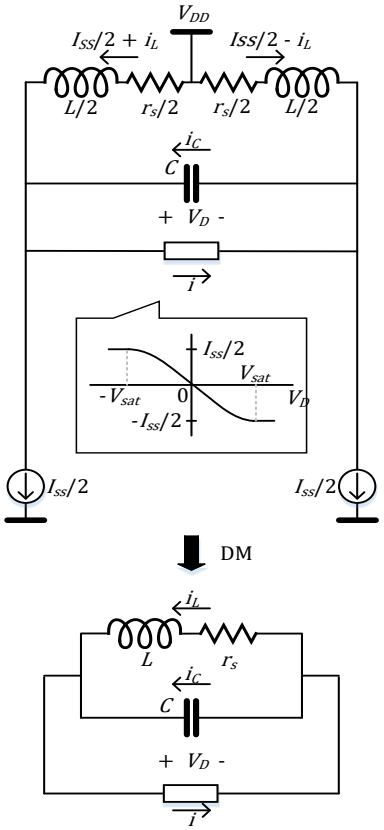

Figure 2. DM equivalent circuit of the CMOS LC oscillator in *figure 1*

The differential-mode (DM) equivalent circuit of the CMOS LC oscillator in *fig. 1* contains the LC tank (where r_s represents the loss resistance of the inductor) and the non-linear voltage controlled current source (VCCS) as illustrated in *fig. 2*. The relationship between i and V_D is given by

$$i = \begin{cases} I_{SS}/2 & ; \quad V_D < -V_{sat} \\ \frac{-g_m V_D}{2}\sqrt{1-\left(\frac{g_m V_D}{2I_{SS}}\right)^2} & ; \quad -V_{sat} < V_D < V_{sat} \\ -I_{SS}/2 & ; \quad V_D > V_{sat} \end{cases} \tag{3}$$

Where

$$V_{sat} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} S}} \tag{4}$$

and

$$g_m = \sqrt{I_{SS}\mu_n C_{ox} S} \tag{5}$$

where S represents the aspect ratio of MOSFET. [8]

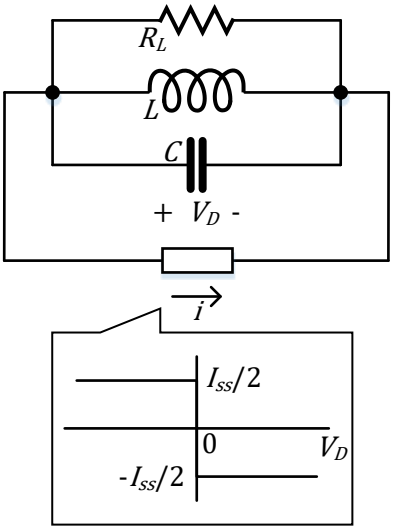

Figure 3. DM equivalent circuit of the oscillator in *fig. 1* at $\omega > \omega_0$ for very high MOSFET transconductance

For frequencies around and higher than the oscillation frequency ω_0 the LC tank in *fig. 2* can be transformed into a parallel RLC network as depicted in *fig. 3* where [see Appendix]

$$R = \frac{L}{r_s C} \tag{6}$$

According to the circuit in *fig. 3*, the impedance of the RLC parallel network can be expressed as

$$Z(s) = \frac{sLR}{s^2 LCR + sL + R} \tag{7}$$

or equivalently

$$Z(j\omega) = \frac{j\omega LR}{R(1-\omega^2 LC) + j\omega L} \tag{8}$$

3. THIRD HARMONIC DISTORTION ANALYSIS

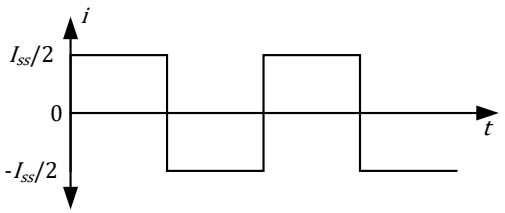

Figure 4. The waveform of the current i in *fig. 3*

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If the MOSFETs in the LC oscillator have very high transconductance (g_m), the characteristic of the cross-coupled differential pair looks like a step function as depicted in *fig. 3*. Although in practice finite transconductance would introduce deviations from an ideal square waveform, the square-wave assumption adopted in the proposed analysis is reasonable, as it reflects the high transconductance of the cross-coupled pair, which is necessary to satisfy the oscillation condition. The square-wave function shown in *fig. 4* has been widely used in the analysis of LC oscillators. For this reason, the square-wave assumption as shown in *fig. 4* has been widely used in the analysis of LC oscillators [9-16]. The square wave can be expressed using Fourier series analysis as

$$i(t) = \frac{2I_{SS}}{\pi}\left(\sin(\omega_0 t) + \frac{\sin(3\omega_0 t)}{3} + \cdots\right) \quad (9)$$

Or $i(t) = I_1 \sin(\omega_0 t) + I_3 \sin(3\omega_0 t) + \cdots$ (10)

Where

$$I_1 = \frac{2I_{SS}}{\pi} \quad (11)$$

and

$$I_3 = \frac{2I_{SS}}{3\pi} \quad (12)$$

I_1 and I_3 are the fundamental and the third harmonic component of i respectively. Referring to *fig. 4* and *eq. (9)* the magnitude of the fundamental component of the voltage V_D can be expressed as

$$V_1 = I_1|Z(j\omega_0)| \quad (13)$$

According to *eq. (2)* and *(8)*

$$|Z(j\omega_0)| = R \quad (14)$$

and by substituting *eq. (12)* and *(14)* into *eq. (13)* we have

$$V_1 = \frac{2I_{SS}}{\pi}R \quad (15)$$

Similarly, by referring to *fig. 4* and *eq. (9)* the magnitude of the third harmonic component of the V_D can be expressed as

$$V_3 = I_3|Z(3j\omega_0)| \quad (16)$$

According to *eq. (2)* and *(8)*

$$|Z(3j\omega_0)| = \sqrt{\frac{1}{\frac{64C}{9L} + \frac{1}{R^2}}} \quad (17)$$

which under the condition $R \gg \sqrt{L/C}$ or equivalent $r_s \ll \sqrt{L/C}$ the above equation can be approximated as

$$|Z(3j\omega_0)| = \frac{3}{8}\sqrt{\frac{L}{C}} \quad (18)$$

By substituting *eq. (12)* and *(18)* into *eq. (16)* we have

$$V_3 = \frac{I_{SS}}{4\pi}\sqrt{\frac{L}{C}} \quad (19)$$

The third harmonic distortion factor HD_3 is given by

$$HD_3 = \frac{V_3}{V_1} \quad (20)$$

Substituting *equations (15)* and *(19)* into *eq. (20)* yields

$$HD_3 = \frac{\sqrt{L/C}}{8R} \quad (21)$$

which can be re-expressed by using *equations (2)* and *(6)* as

$$HD_3 = \frac{1}{8\omega_0}\left(\frac{r_s}{L}\right) \quad (22)$$

where the factor r_s/L is dependent on the process parameter and ω_0 is a specification parameter of the oscillator.

4. SIMULATION RESULTS

To verify the proposed analysis, the CMOS LC oscillator shown in *fig. 1* was simulated using the Spectre circuit simulator in LTspice with the TSMC 0.18-micron CMOS process technology and a V_{DD} of 3 V. The inductance parameters were set to L = 44 nH and r_s = 20 Ω [16], and capacitance values from 2 pF to 10 pF were used.

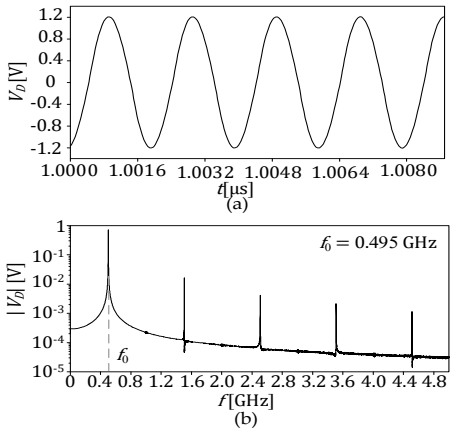

Figure 5. Output voltage of the oscillator in *fig. 1* for C = 2 pF where (a) waveform and (b) FFT spectrum, showing a fundamental frequency of 0.495 GHz and the presence of harmonic components

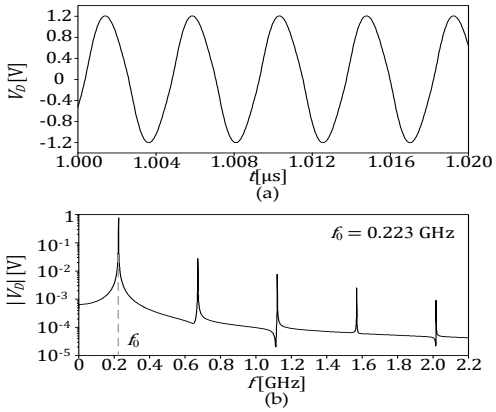

Figure 6. Output voltage of the oscillator in Fig. 1 for C = 10 pF where (a) waveform and (b) FFT spectrum, showing a fundamental frequency of 0.223 GHz and the presence of harmonic components

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To maintain an oscillation voltage of approximately 1.2 V, the corresponding tail currents were set from 2.0 mA (for C = 2 pF) to 9.0 mA (for C = 10 pF). The waveform and FFT of the output voltage for C = 2 pF and C = 10 pF are shown in *fig. 5* and *fig. 6*, respectively.

Table 1. Comparison of simulation and analytical results of the third harmonic distortion for transistor dimensions W/L = 100µ/0.2µ for M_0, M_1 and M_2

C [pF]	f_0 [GHz]	HD_3 sim. [%]	HD_3 Ana. [%]	Error [%]
2.0	0.495	2.03	1.83	9.9
3.0	0.411	2.20	2.20	0.1
4.0	0.358	2.46	2.53	2.7
5.0	0.321	2.72	2.82	3.7
6.0	0.292	2.96	3.09	4.6
7.0	0.270	3.18	3.35	5.5
8.0	0.252	3.37	3.60	6.8
9.0	0.236	3.59	3.83	6.6
10.0	0.223	3.78	4.05	7.2

Table 2. Comparison of simulation and analytical results of the third harmonic distortion for transistor dimensions W/L = 100µ/0.2µ for M_0 and W/L = 80µ/0.2µ for M_1 and M_2

C [pF]	f_0 [GHz]	HD_3 sim. [%]	HD_3 Ana. [%]	Error [%]
2.0	0.502	1.92	1.80	5.9
3.0	0.415	2.15	2.18	1.6
4.0	0.36	2.42	2.51	3.9
5.0	0.323	2.70	2.80	3.9
6.0	0.293	2.91	3.09	6.2
7.0	0.271	3.16	3.34	5.5
8.0	0.253	3.32	3.58	7.9
9.0	0.237	3.50	3.81	8.9
10.0	0.224	3.69	4.03	9.4

Table 3. Comparison of simulation and analytical results of the third harmonic distortion for transistor dimensions W/L = 80µ/0.2µ for M_0 and W/L = 100µ/0.2µ for M_1 and M_2

C [pF]	f_0 [GHz]	HD_3 sim. [%]	HD_3 Ana. [%]	Error [%]
2	0.495	2.03	1.83	10.1
3	0.411	2.23	2.20	1.5
4	0.358	2.50	2.53	1.2
5	0.320	2.71	2.82	4.2
6	0.292	2.98	3.04	2.0
7	0.270	3.17	3.35	5.6
8	0.252	3.39	3.59	6.0
9	0.236	3.62	3.82	5.7
10	0.223	3.82	4.05	6.2

Table 4. Comparison of simulation and analytical results of the third harmonic distortion for transistor dimensions W/L = 80µ/0.2µ for M_0, M_1 and M_2

C [pF]	*f0 [GHz]*	*HD3 sim. [%]*	*HD3 Ana. [%]*	*Error [%]*
2	0.502	1.92	1.80	6.2
3	0.415	2.15	2.18	1.6
4	0.361	2.43	2.51	3.0
5	0.323	2.67	2.80	4.9
6	0.294	2.90	3.08	6.1
7	0.271	3.13	3.33	6.7
8	0.253	3.32	3.58	7.9
9	0.237	3.56	3.81	7.1
10	0.224	3.63	4.03	11.2

Tables 1–4 summarize the comparison between the analytical and simulation results of HD_3 for different transistor dimension conditions of M_0, M_1, and M_2. In all cases, the analytical results are close to the simulation data over the investigated frequency range. For clearer visualization, the corresponding comparisons are plotted in *fig. 7*.

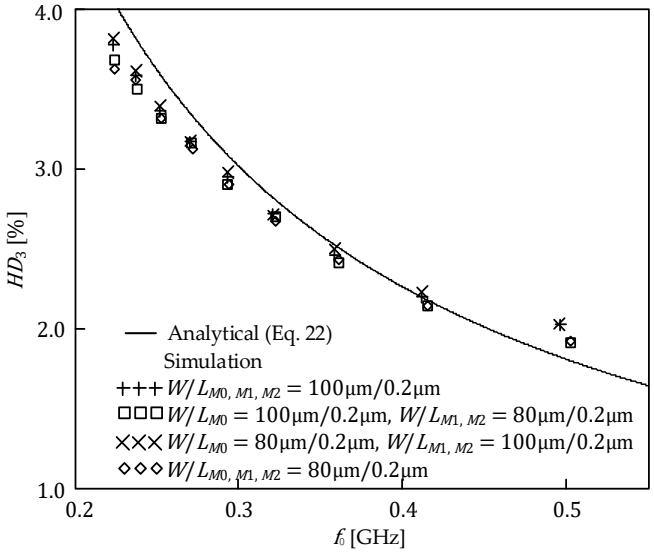

Figure 7. Comparison of analytical (*eq. 22*) and simulation results of HD_3 under different transistor sizing conditions. Simulation markers correspond to capacitance values from 2 pF to 10 pF.

It can be observed from *fig. 7* that the predicted values of HD_3 are close to simulation results except at higher frequency range close to 0.5 GHz in which the simulation results exceed the theoretical results due to parasitic components of the MOS devices not accounted for in the analysis. This deviation is mainly caused by neglected parasitic effects of the MOS devices, which become more pronounced at higher frequencies. From *eq. (22)*, it can be observed that the HD_3 depends on the r_s/L ratio. To minimize the r_s/L ratio of an on-chip inductor, several design strategies can be applied. The

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parasitic resistance r_s can be reduced by using the thick top metal layer available in the CMOS process, increasing the width of the metal traces, and employing stacked metal layers connected with vias to lower the effective series resistance [17]. In addition, optimizing the spiral geometry, such as using circular or octagonal layouts, and reducing unnecessary conductor length can further decrease resistance. Techniques such as increasing the spacing between turns and using patterned ground shields can also help reduce substrate losses and proximity effects. These approaches collectively reduce the effective resistance of the inductor while maintaining the desired inductance value, thereby improving the overall performance of the LC tank circuit.

5. CONCLUSIONS

An analytical method for evaluating HD_3 in CMOS LC oscillators has been presented, in which a closed-form expression is derived and validated through simulation, showing good agreement with acceptable error. The results highlight the dependence of HD_3 on the r_s/L ratio, which is closely related to the quality factor of the inductor, thereby providing useful design insight. The proposed method offers a straightforward and efficient approach for distortion analysis in high-purity oscillator design.

Appendix A

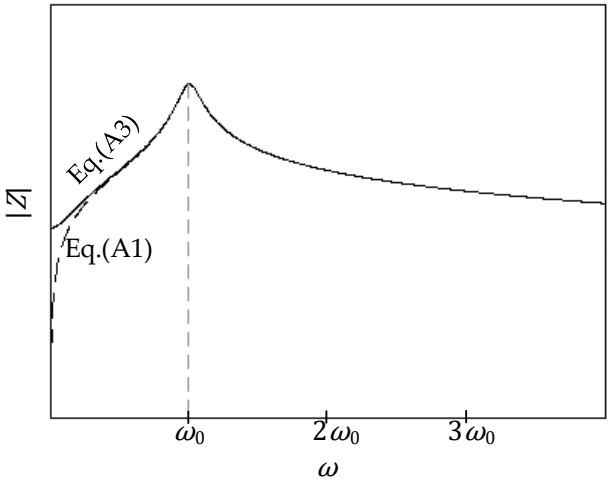

Figure A1. HD_3 comparison of the results of calculations and simulations AC responses of impedance functions in *eq. (A1)* and (A3)

The impedance of the DM LC tank in *fig. 2* may be determined by using an ac analysis, and the result is

$$Z(j\omega) = \frac{j\omega L + r_s}{(j\omega)^2 LC + j\omega C r_s + 1} \quad \text{(A1)}$$

However, at frequencies near and above oscillation frequency, ω_0, Z is equation (A1) can be approximated as

$$Z(j\omega) \approx \frac{j\omega L}{(j\omega)^2 LC + j\omega C r_s + 1} \quad \text{(A2)}$$

By rearranging *eq. (A2)*, we obtain

$$Z(j\omega) \approx \frac{1}{j\omega C + \frac{1}{j\omega L} + \frac{1}{R}} \quad \text{(A3)}$$

Where

$$R = \frac{L}{r_s C} \quad \text{(A4)}$$

which is equivalent to *fig. 3's* LRC parallel network.

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Conflicts of Interest: "The authors declare no conflict of interest."

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