

Improved JAYA Optimization Based Adaptive Controller for UPQC to Solve Power Quality Issues

B Pavankumar¹, and Saroj Padhan^{2*}

¹Department of Electrical Engineering, PMEC, Biju Pattanik University and Technology, Odisha, India; e-mail: bpavan220@gmail.com

²Department of Electrical Engineering, PMEC, Biju Pattanik University and Technology, Odisha, India; e-mail: saroj.ee@pmec.ac.in

*Correspondence: Saroj Padhan, saroj.ee@pmec.ac.in

ABSTRACT- Power quality issues in distribution system network adversely affect the performance of modern power distribution systems. Although several compensation techniques have been reported in the literature to solve this problem, most of them address to solve voltage leads power quality and current leads power quality issues independently. However, this paper focuses on power quality issues raised by both voltage and current simultaneously. In this a Unified Power Quality Conditioner has been proposed to solve these issues. The proposed UPQC consists of a common DC link with a Series Active Power Filter and a Shunt Active Power Filter. The main contribution of this work is the development of an Improved JAYA (IJAYA) optimization-based adaptive control strategy for accurate reference signal generation and effective DC-link voltage regulation. The IJAYA algorithm optimally tunes the proportional-integral (PI) controller gains by minimizing the mean square error (MSE), resulting in rapid convergence to the optimal gain values and stable DC-link voltage operation. The optimized gains converge to $K_p=1.3$ and $K_i=0.26$. The SEAPF employs an Enhanced Phase-Locked Loop and Synchronous Reference Frame control technique for reference voltage generation, whereas the SAPF utilizes active component estimation and Unit Vector Template Generation techniques for reference current generation. Simulation results show very encouraging as the Total Harmonic Distortion (THD) level reduced to 2.10%, 3.35%, and 3.62% of the fundamental under sag, swell, and harmonic conditions, respectively. These values satisfy the IEEE 519 standard requirements, confirming the suitability of the proposed UPQC for modern power distribution networks.

Keywords: Power Quality, Unified Power Quality Conditioner, Improved JAYA, Proportional Integral Controller, Synchronous Reference Frame, Enhanced Phase Locked Loop.

ARTICLE INFORMATION

Author(s): B Pavankumar, and Saroj Padhan;

Received: 08/04/26; **Accepted:** 12/06/26; **Published:** 30/09/26;

E- ISSN: 2347-470X;

Paper Id: IJEER 0804B04;

Citation: 10.37391/ijeer.140303

Webpage-link:

<https://ijeer.forexjournal.co.in/archive/volume-14/ijeer-140303.html>



Publisher's Note: FOREX Publication stays neutral with regard to jurisdictional claims in Published maps and institutional affiliations.

including switching transients, harmonic injection, and advanced control requirements [1–2].

Over the past few decades, various power conditioning and filtering techniques have been used to solve these issues. Initially, passive filters were widely employed for harmonic mitigation; however, their effectiveness was limited by fixed compensation characteristics and resonance-related problems. To overcome these limitations, active power filters and custom power devices were introduced. Among these devices, the Unified Power Quality Conditioner (UPQC) mainly design to solve power quality issues raises due to both voltage and current, whereas Dynamic Voltage Restorer (DVR) and Distribution Static Compensator (DSTATCOM) designed to solve voltage and current problem independently [2–3].

The Unified Power Quality Conditioner (UPQC) is one of the most effective custom power devices for mitigating multiple power quality disturbances simultaneously. It is capable of compensating for voltage imbalance, harmonics, reactive power demand, and negative-sequence currents through the coordinated operation of its series and shunt active filters. Various UPQC configurations and control strategies have been reported in the literature, demonstrating improved adaptability and performance under different operating conditions. Recent research trends indicate a growing emphasis on voltage issues

1. INTRODUCTION

Power electronic devices, automated systems, and digital equipment are extensively used in modern industrial applications. These devices generally operate as nonlinear loads and introduce distortions into the power system, resulting in power quality (PQ) issues. These disturbances degrade system performance and efficiency, adversely affect sensitive equipment, increase operating costs, and may lead to malfunction or instability in system operation and control. Furthermore, the increasing integration of renewable energy systems such as wind and photovoltaic (PV) generation, has intensified these challenges. Although DG systems contribute significantly to sustainable energy development, their power electronic interfaces introduce additional complexities,

compensation, harmonic mitigation, and the application of advance techniques for power quality monitoring and enhancement. In addition, considerable attention has been devoted to the development of comprehensive, intelligent, and scalable solutions for power quality improvement [3–5]. Under nonlinear load and disturbed supply conditions, the UPQC provides effective compensation for power quality problems, thereby improving system reliability, enhancing equipment lifespan, increasing operational efficiency, and ensuring compliance with IEEE power quality standards [6].

Several researchers have proposed different UPQC configurations and control strategies to improve compensation performance and reduce implementation cost. In [7], a transformer-less UPQC was proposed to achieve enhanced compensation capability, reduced cost, and simplified control implementation. Similarly, optimization-based approaches have been employed in [8] to minimize the rating and cost of UPQC systems by integrating advanced optimization algorithms with superconducting fault current limiters (SFCLs). A hybrid artificial intelligence-based optimization approach was presented in [9], demonstrating improved dynamic performance and reduced design cost. In addition, enhanced classical proportional-integral (PI) controllers optimized using techniques such as genetic algorithms have been reported to provide significant performance improvements [13]. In [14], a digital filter based on voltage identification for damping of harmonic was proposed and the work is validated through experimental analysis. Furthermore, a fuzzy logic controller (FLC)-based UPQC with a low-rating series compensator was presented in [10], which effectively mitigates voltage sags and improves the power factor. A UPQC with UVT and PI combine controller has been proposed [11], where both simulation and experimental results demonstrated its capability to simultaneously compensate voltage and current distortions.

The development of an effective control strategy for generating appropriate switching signals leads to achieving satisfactory compensation performance. Various control methodologies have been reported for the Series Active Power Filter (SEAPF) and Shunt Active Power Filter (SAPF) sections of the UPQC [12–19]. A Static Synchronous Compensator (STATCOM)-based approach was presented in [13] to address voltage-related power quality disturbances. Furthermore, JAYA- and Modified JAYA-based optimized PI controllers integrated with indirect control techniques have been implemented in Dynamic Voltage Restorers (DVRs) to improve voltage compensation capability. For current-related power quality improvement, SRF control combined with BAT optimization was proposed in [14], while JAYA- and Modified JAYA-based control strategies were employed in SAPF applications to enhance current harmonic compensation performance [15–16]. In addition, adaptive hysteresis band controllers with different control schemes have been reported for generating switching signals and improving converter performance [17–18]. Separate voltage and current hysteresis controllers for series and shunt converters were presented in [19] to achieve effective switching control. Although these approaches have demonstrated satisfactory performance in

addressing specific power quality issues, limited attention has been given to the coordinated integration of Improved JAYA optimization with SRF-, PLL-, Active Component Estimation, and Unit Vector Template Generation (UVTG)-based techniques within a unified UPQC control framework. This limitation motivates the development of the proposed control strategy.

1.1. Reserch Gap and Contribution

The literature survey provides several approaches for enhancing power quality using techniques such as JAYA optimization, Synchronous Reference Frame (SRF) control, Phase-Locked Loop (PLL), Shunt Active Power Filters (SAPF), and Series Active Power Filters (SEAPF). Although these methods have demonstrated satisfactory performance in mitigating power quality disturbances, most existing studies focus on the individual application of these techniques. Furthermore, only a limited number of studies have employed JAYA-based optimization for tuning PI controller parameters in UPQC applications. The coordinated integration of an Improved JAYA optimization algorithm with SRF- and PLL-based control strategies for both series and shunt converters of a UPQC has not been adequately investigated. Therefore, a research gap exists in developing an integrated control structure capable of simultaneously improving reference signal generation accuracy, controller tuning, and compensation performance under multiple power quality issues.

To address this gap, the present work proposes an Improved JAYA optimization-based control methodology for a Unified Power Quality Conditioner (UPQC). In the series compensation path, the Improved JAYA-optimized PI controller is integrated with SRF and PLL techniques to generate accurate voltage reference signals for effective voltage compensation. In the shunt compensation path, the same optimization control methodology is combined with Active Component Estimation, Unit Vector Template Generation (UVTG), and PLL techniques to generate precise current reference signals. In addition, adaptive hysteresis voltage and current controllers are employed in the series and shunt converters, respectively, to achieve effective switching control and improved compensation performance.

The main contributions of the proposed work are

1. Development of an Improved JAYA-based optimization structure for optimal tuning of PI controller parameters in UPQC applications.
2. Integration of Improved JAYA optimization with SRF, PLL, Active Component Estimation, and UVTG techniques for accurate voltage and current reference signal generation.
3. Implementation of adaptive hysteresis voltage and current controllers to enhance switching performance and compensation capability.
4. Simultaneous mitigation of power quality issues raised due to voltage and current through coordinated control of the series and shunt converters.
5. Improvement in control accuracy, DC-link voltage regulation, and overall power quality enhancement while maintaining compliance with IEEE 519 harmonic standards.

2. DESCRIPTION OF PROPOSED WORK

Figure 1 illustrates the system setup, which is a three-phase supply with a voltage magnitude of 380 V and a frequency of 50 Hz. This supply is fed to a non-linear load comprising resistive and inductive components along with a diode bridge rectifier. It is well known that such non-linear loads degrade overall power quality by introducing harmonics and waveform distortions.

To enable proper voltage injection, the SEAPF is connected on the supply side through R-L filters and a boosting transformer. SAPF is connected in parallel through R-L filter for injection of compensating current. Both the SEAPF and SAPF are implemented using voltage source converters (VSCs), each comprising six Insulated Gate Bipolar Transistors (IGBTs), to facilitate accurate and fast switching operations. The used parameters in the design of UPQC and its values are presented in table 1. The system is designed with suitable control methodology to improve the overall performance of a distribution network by reducing the power quality issues raised due to both voltage and current.

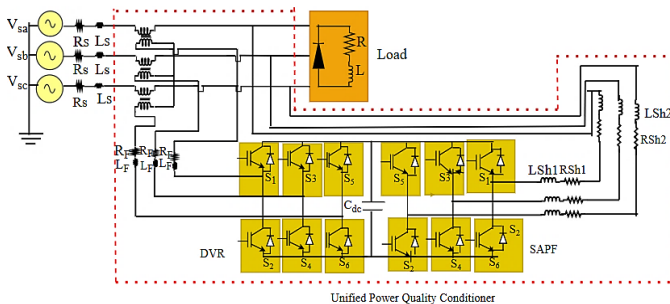


Figure 1. Proposed system with UPQC

Table 1. Parameters used and its values

S. No.	Parameters	Values
1	Grid voltage	380 V (L-L), 50 Hz, 3-Phase
2	Source Impedance	1.5Ω, 0.5mH
3	Filter Coupling Impedance	1.8Ω, 1.5mH
4	Load Parameter	R = 60Ω, L = 20mH
5	DC Link voltage	760V
6	Optimized Gain	1.2 [L-0.1-2.0-H], 0.26[L-0.01-0.1-H]
7	Switching Frequency	10kHz
8	Load rating	2.38kw

3. DEVELOPMENT OF CONTROLLER

The development of the controller is essential for accurate reference signal generation and improved switching pulse generation for the voltage source inverters associated with the proposed UPQC. Separate methodologies for controlling

action of the converters are employed for the SEAPF and SAPF. However, since both conditioners are regulated through a common DC-link voltage, a modified JAYA optimization algorithm [13], [15] is utilized to optimize the gains and minimize the control error. The regulated output of the PI controller is then integrated with other control techniques [14], [16] – [19] to generate accurate switching signals for the injection of compensating voltages and currents. The steps involved in the proposed control methodology are described as follow.

3.1. Enhanced Phase Locked Loop

An Enhanced Phase-Locked Loop (EPLL) is used in the control strategy to precisely synchronize with the grid voltage. Even when the supply voltage's phase angle and frequency vary significantly, the EPLL helps synchronize and keeps the dq transformation's reference frame.

3.2. Developed Modified Jaya

In the conventional JAYA optimization technique [13], [15], the best and worst solutions are identified from the entire population. However, this approach may adversely affect the PI controller's output performance and require a greater number of iterations to achieve convergence. To further enhance performance, a modification is introduced to the JAYA algorithm, resulting in an Improved JAYA (IJAYA) optimization technique. The proposed modification improves the quality of the reference output when combined with the other control techniques. In the IJAYA algorithm, the population is first arranged in descending order from the best to the worst solution [13] and subsequently divided into two groups: the best and worst solution group. The term "Best" denotes the best solution within the best solution group, whereas "Worst" denotes the best solution within the worst solution group. This strategy reduces the iterations number required to obtain an optimized solution. The modifications introduced in the optimization process are described below, and the corresponding flowchart is presented in fig. 2.

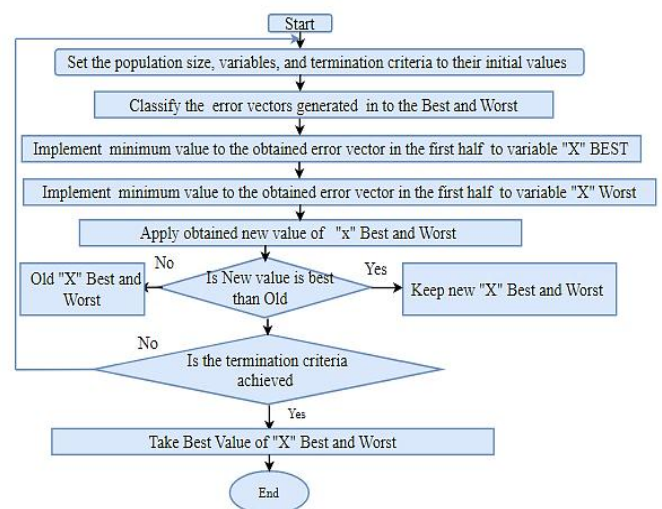


Figure 2. Proposed modified IJAYA optimized flow chart

Algorithm 1: Proposed IJAYA Optimization Algorithm

Initialize population size(n), design variables(K_p, K_i, L, C), search bounds (L_b, U_b) and maximum iterations.

Generate the initial population randomly within the specified bounds.
Select the objective function (J) for all candidate solutions.

Rank the candidate solutions according to the objective function values.

Divide the ranked population into best and worst groups.

Select the minimum-error solution from the two groups as ("X"Best) and ("X"Worst).

Update the candidate solutions using the IJAYA update equation.

Evaluate the updated solutions and compare them with the previous solutions.

Retain the better solutions for the next iteration.

*Check the termination criterion:
if satisfied, proceed to Step 12.
Otherwise, return to Step 4.*

Obtain the optimal values of (K_p) , (K_i) , and (L, C)
 Generate the optimized control signal for UPOC operation.

At first, initialize the population size, optimization variables, and termination criteria. The generated error vectors are then ranked and divided into Best and Worst groups. The minimum-error candidate from the Best group is assigned ("X $_{Best}$ "), while the minimum error candidate from the Worst group is assigned to ("X $_{Worst}$ "). These candidates are subsequently used to update the solution vectors in each iteration, compared with previous one and the superior candidates are retained for the next iteration. This process going on till termination criterion is satisfied, after which the optimal solution is selected.

The IJAYA is used to determine the optimal values of gains (K_p, K_i) of the PI controller and the coupling inductor parameter (L, C) within the specified search bounds. The optimization process aims to minimize the simulation-based error using the Mean Square Error (MSE) objective function.

$$\text{Considered objective function } J = \sum_{i=1}^{ITER} E_r^2 \quad (1)$$

Jaya algorithm is used here to tune (K_p, K_i, L, C) within defined bounds to minimize simulation-based error

Chosen population size: $n=10$;

Selected Parameter: $d=4$:

Parameters lower and upper bounds are represented as L_b, U_b

Selected values of $L_b = [1 \ 0 \ 0 \ 0]$ and $U_b =$

$$[1000 \quad 1000 \quad 1000 \quad 1000]$$

Maximum iteration set for 50 iterations, thereby error is minimized by

$$MSE(i) = \left(\frac{Error^2}{n} \right) \quad (2)$$

In the proposed IJAYA algorithm, the population is first ranked according to the objective function value and then divided into Best and Worst groups. The minimum error candidate from the Best group is assigned as $(X^{Best})_{X_{Best}} - (X^{Best})_X$, while the minimum error candidate from the Worst group is assigned as $(X^{Worst})_{X_{Worst}} - (X^{Worst})_X$. These solutions are utilized to update the search vectors, thereby improving convergence speed and reducing computational effort.

3.3. Reference voltage generation

The reference voltage signal is generated using the proposed controller integrated with the IJAYA optimization technique, as illustrated in *fig. 3*. Initially, the optimized output obtained from the IJAYA algorithm is combined with the SRF-based control scheme to enhance the reference signal generation process. The EPLL continuously tracks the three-phase supply voltages and provides the phase angle required for synchronization. The measured three-phase voltages are transformed into the synchronous rotating dq reference frame using Park's transformation. The EPLL maintains accurate reference frame alignment even under variations in the supply voltage phase angle and frequency. After processing in the dq frame, the signals are transformed back to the abc frame through the inverse Park's transformation. A low-pass filter (LPF) is employed to eliminate high-frequency ripple components and obtain smooth reference signals. The SRF-based voltage extraction process is represented by the Park's transformation given in *eq. (3)*.

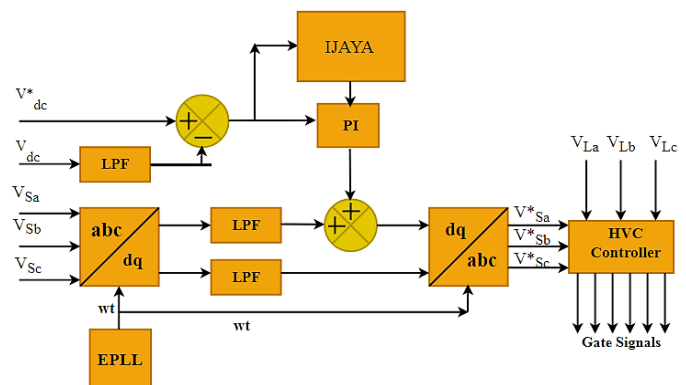


Figure 4. Reference signal generation for current sign

$$\begin{bmatrix} V_{Sa}^* \\ V_{Sb}^* \\ V_{Sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & -\sin \theta & 1 \\ \cos(\theta - 120^\circ) & \sin(\theta - 120^\circ) & 1 \\ \cos(\theta + 120^\circ) & \sin(\theta + 120^\circ) & 1 \end{bmatrix} \begin{bmatrix} V_{sd} \\ V_{sq} \\ V_0 \end{bmatrix} \quad (3)$$

Where $V_{Sa}^*, V_{Sb}^*, V_{Sc}^*$ denote the reference phase voltages, and θ is the phase angle obtained from the EPLL.

3.3. Reference current generation

The reference current signals are generated using the Active Component Technique, the Novel Instantaneous Reactive Power Theory based controller, and the Unit Vector Template Generator (UVTG), together with the optimized output obtained from the IJAYA algorithm, as shown in *fig. 4*. The load currents are processed to extract the active and reactive current components required for compensation. The UVTG

provides synchronized unit templates, while the IJAYA-optimized signal improves the accuracy of the generated reference currents. The mathematical representation of the reference current generation is given in eq. (4).

The generated reference voltage and current signals are applied to the hysteresis voltage and current controllers [24], [25] to produce the switching pulses for the voltage source converters. These switching signals enable the injection of compensating voltages and currents, thereby mitigating power quality disturbances and improving the overall performance of the UPQC [26]–[28].

$$\begin{bmatrix} I_{sa}^* \\ I_{sb}^* \\ I_{sc}^* \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & 0 \\ -1 & \frac{\sqrt{2}}{2} \\ -1 & -\frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (4)$$

Where I_{sa}^* , I_{sb}^* , I_{sc}^* denote the reference phase voltages, and θ is the phase angle obtained from the EPLL.

4. RESULT AND ANALYSIS

The developed controller is implemented in both the series and shunt components of the proposed UPQC, and the system performance is analyzed using the MATLAB/Simulink environment.

4.1. Analysis of Optimized Gain of the PI Controller and Regulated Common DC Link Voltage

From the obtained mean square error *figure 7*, it can be observed with a K_p value of 1.2 and a K_i value of 0.25, the first iteration began with a value of 409.8101. In the second iteration, the improved Jaya method demonstrated its highest performance with K_p and K_i reductions of 1.2103 and 0.2692, respectively, and operated 100% efficiently in lowering the MSE to 204.9. Ten iterations later, the MSE drops to 36.3, K_p is 1.2, and K_i is 0.27. MSE decreases to 13.2 after thirty iterations and stays at that level for forty iterations. The integral constant and proportional constant are reduced to 0.26 and 1.2, respectively. *figure 5* and *figure 6*. shows the results of IJAYA optimization's convergence, the algorithm's behavior when adjusting PI controller gains (K_p and K_i), and the convergence charts confirm the process's efficiency, speed, and stability. The DC regulate voltage without IJAYA and with IJAYA are presented in *figure 8* and *figure 9* respectively.

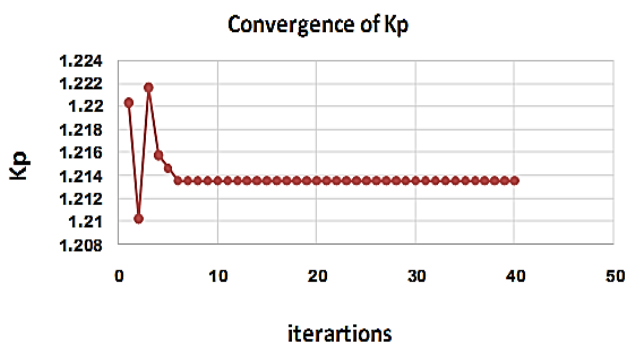


Figure 5. Convergence of K_p

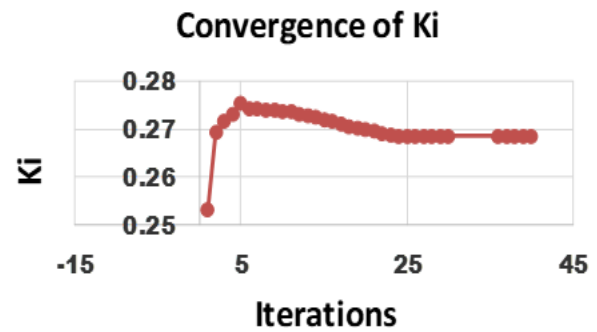


Figure 6. Convergence of K_i

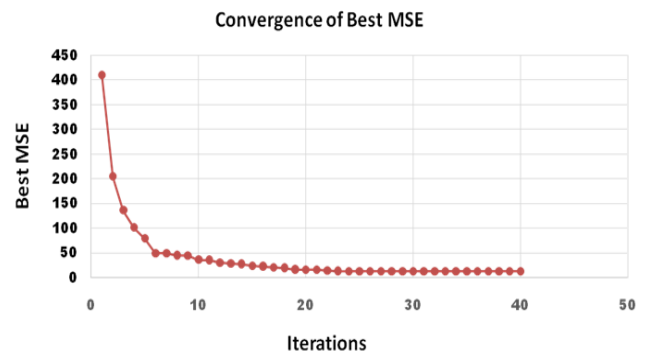


Figure 7. Convergence of Best MSE

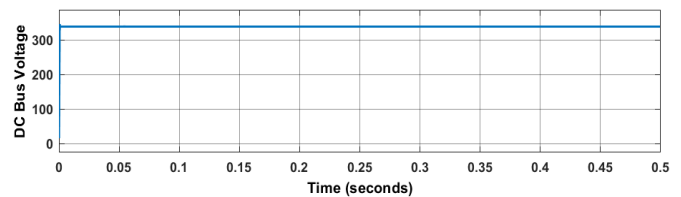


Figure 7. DC regulated without IJAYA

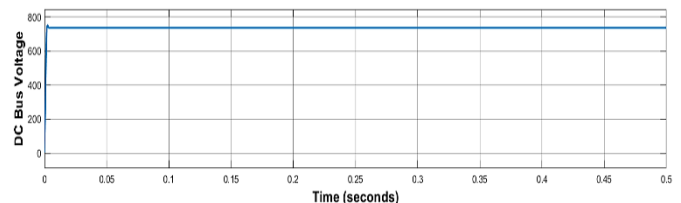


Figure 9. DC regulated voltage with IJAYA

4.2. Verification of Voltage Sag-Swell Compensation and its analysis

When a dual voltage sag occurs at the source side, the voltage amplitude is reduced by up to 20% of its nominal value. This reduction in the supply voltage is directly reflected at the load side, causing a corresponding decrease in the load voltage amplitude. Such deviations from the nominal voltage may lead to abnormal operation of the connected loads and adversely affect system performance. To mitigate these effects and maintain the load voltage at the desired level, the UPQC operates by injecting the required compensating voltage during the sag condition.

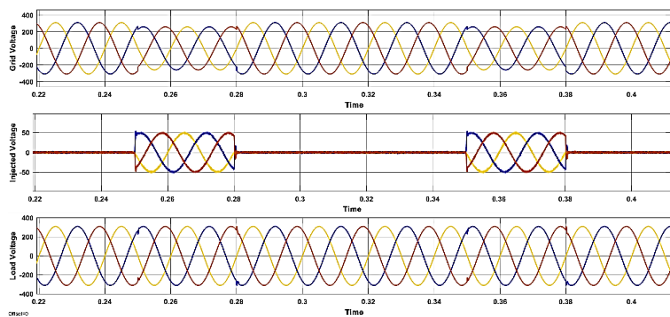


Figure 10. (a) Grid voltage with double sag (b) Injected voltage from the SEAPF (c) Load voltage after injection

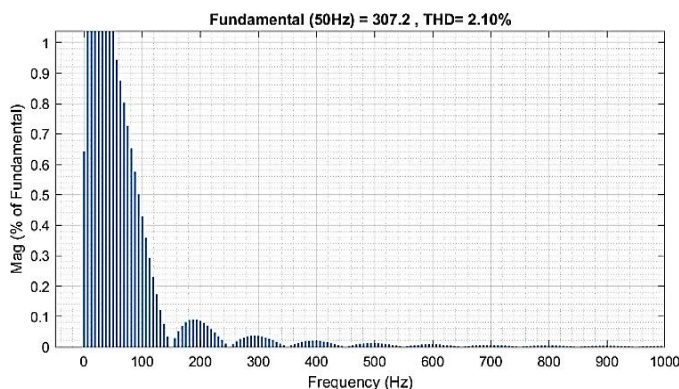


Figure 11. THD analysis after Injection of UPQC

The figure 10(a) shows the occurrence of dual voltage sags in the source voltages from 0.25s to 0.28s and from 0.35 s to 0.38 s. For the elimination of these voltage sags, injection voltage signals are generated by the UPQC using the proposed controller, as presented in figure 10(b). These injection signals mitigate the voltage sags and regulate the load voltage, as shown in figure 10(c), thereby ensuring a stable supply for the consumer loads. This behavior protects the connected loads from abnormal operation and enhances their service life.

The voltage distortion THD analysis is presented in figure 11. After compensation, the THD level is reduced to 2.10% of the fundamental component, whereas the THD before compensation was 12.61%. The obtained THD value is within the acceptable limits specified by IEEE standards.

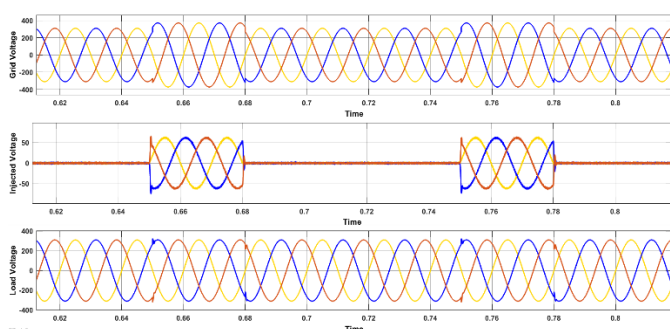


Figure 12. (a) Grid voltage with double sag (b) Injected voltage from the SEAPF (c) Load voltage after injection

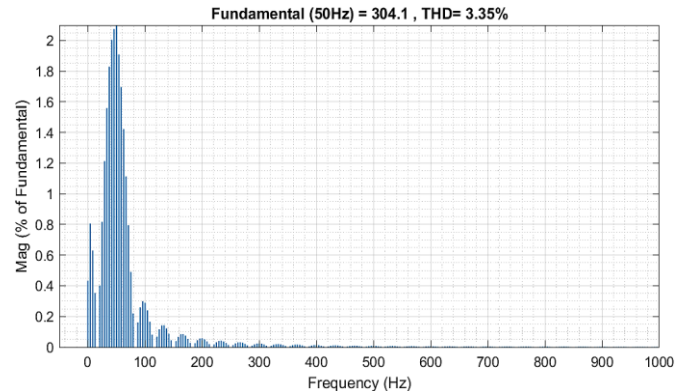


Figure 13. THD analysis after Injection of UPQC

Similarly, under voltage swell conditions, the amplitude of the source voltage increases by 20% to 30% above its nominal value. Figure 12(a) shows the occurrence of dual voltage swells from 0.65 s to 0.68 s and from 0.75 s to 0.78 s. The observed swell corresponds to a 20% increase in the amplitude of the source voltage. To compensate for this disturbance, the UPQC employing the proposed controller generates the compensating signal shown in figure 12(b). As a result, the regulated load voltage is maintained, as presented in figure 12(c).

The voltage distortion THD analysis is presented in Figure 15. After compensation, the THD level is reduced to 3.35%, whereas the THD before compensation was 12.61% of the fundamental component. The obtained THD value is within the acceptable limits specified by IEEE standards.

4.3. Analysis of Harmonics Compensation

The harmonic distorted source voltage and load current under nonlinear load conditions are shown in figures 14(a) and 14(b), respectively. The load current is highly distorted due to the presence of harmonics. These current harmonics are compensated by the shunt part of the UPQC, as shown in figure 14(c). After the injection of the compensating current, the source current becomes nearly sinusoidal, as presented in figure 14(d). The current distortion THD is reduced from 22.28% to 3.62%, as shown in figure 15.

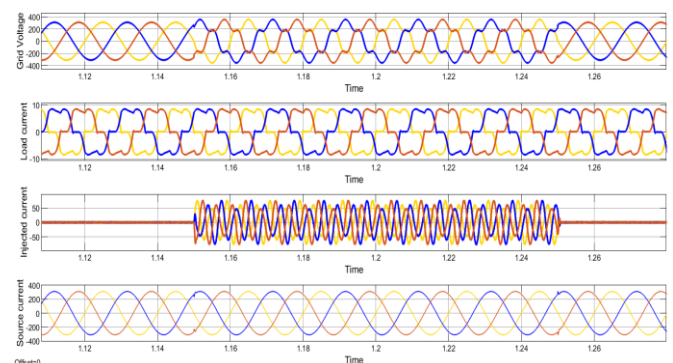


Figure 14. (a) Grid voltage with Harmonics (b) Source Current (c) Compensated current (d) Source current

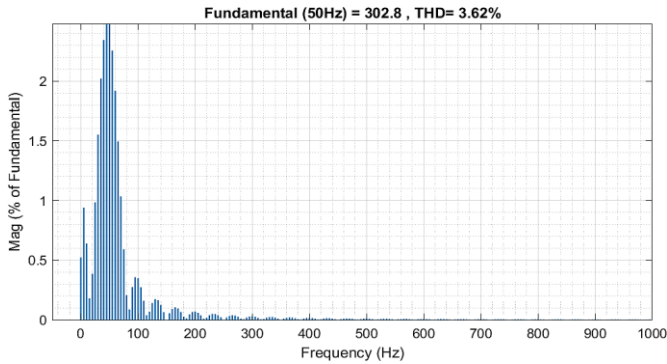


Figure 15. THD analysis after Injection of UPQC

The THD analysis of the above three cases of voltage sag, voltage swell and harmonics are presented in *table 2*.

Table 2. THD Analysis

Power Quality Issues	THD Before Compensation (%)	THD After Compensation (%)	IEEE-519 Limit (%)	Status
Voltage sag	12.61	2.10	<5	Complies
Voltage swell	12.61	3.35	<5	Complies
Harmonics	22.28	3.62	<5	Complies

5. CONCLUSIONS

Due to the growing demand of sensitive and nonlinear loads, power quality enhancement utilizing a UPQC is a crucial requirement in modern distribution systems. In order to reduce power quality problem caused by both voltage and current simultaneously, UPQC comprising a SEAPF and a SAPF coupled with a common DC-link capacitor has been developed in this work. To control the DC-link voltage and enhance overall control performance, an Improved JAYA (IJAYA)-based PI optimization technique has been utilized. While active component extraction, IPRT, and UVTG techniques are used in the shunt compensator for accurate reference signal generation, the improved controller is coupled with Enhanced PLL and SRF techniques in the series compensator.

Voltage sag, voltage swell, and harmonics are considered the operational circumstances in which the efficacy of the suggested UPQC has been observed. The simulation results show that the suggested control technique effectively reduces these issues and keeps the THD under the 5% IEEE 519 recommended limit. The dynamic response and harmonic correction performance are greatly enhanced by the suggested controller

The present work has not taken into account practical implementation concerns such as measurement noise, parameter uncertainties, and communication delays, furthermore; there has been no experimental validation of the suggested controller's performance on a hardware platform.

Future work will concentrate on experimental validation of the suggested UPQC controller under various grid settings and real-time hardware implementation.

REFERENCES

- [1] V.manoj, P.Khampariva, R.Pilla, "A review on techniques for improving power quality: research gaps and emerging trends", Bulletin of Electrical Engineering and Informatics, 2022, vol.11,pp. 3099-3107
- [2] Mbuli, N, " Dynamic Voltage Restorer as a Solution to Voltage Problems in Power Systems: Focus on Sags, Swells and Steady Fluctuations" . Energies, 2023, vol. 16,pp. 6946
- [3] S.Mishra and P.K. Ray "Power Quality Improvement Using Photovoltaic fed DSTATCOM based on JAYA Optimization" IEEE Transactions on Sustainable Energy, 2016, vol. 7, no. 4, pp. 1672-1680
- [4] A.Heenkenda, A. Elsanabar, M. Seyedmahmoudian, et al.; "Unified Power Quality Conditioners Based Different Structural Arrangements: A Comprehensive Review", IEEE Access, 2023, vol. 11, pp. 43435 – 43457
- [5] H. Fujita and H. Akagi, "The Unified Power Quality Conditioner: The integration of shunt and series filters." IEEE Trans on Power Electron, 1998, vol.13, no.2, pp. 315-322
- [6] Y.K.Latha, Ch.saibabu, Y.P.Obselu, "Unified Power Quality Conditioner for Voltage Sag and Harmonic Mitigation of Nonlinear Loads", International Journal of Power Electronics and Drive System (IJPEDS) 201, vol.1, pp. 65-74
- [7] Han, B. Bae "New Configuration of UPQC for Medium-Voltage Application" IEEE Trans on Power Delivery, 2026, vol.21, pp. 1438-1444
- [8] Heydari, Hossein, and Amir Hassan Moghadasi. "Optimization Scheme in Combinatorial UPQC and SFCL Using Normalized Simulated annealing", IEEE Transactions on Power Delivery, 2011, vol.26, pp.1489-1498
- [9] Ramesh Rudraram, Sasi Chinnathamb and Manikandan Mani "PV Integrated UPQC with Intelligent Control Techniques for Power Quality Enhancement, International Journal of Electrical and Electronics Research (IJEER), Forex, 2023, vol. 11, Pages 202-212
- [10]S. P. Thota and S. K. Peddapelli, "Fuzzy Controller based Interline Unified Power Quality Conditioner (IUPQC) in Multi-feeder Systems," 2019 International Conference on Engineering, Science, and Industrial Applications (ICESI), 2019, Tokyo, Japan, pp. 1-5
- [11]Sachin B. Shahapure, Vandana A. Kulkarni and Ramchandra P. Hasabe, Performance Analysis of Renewable Integrated UPQC, International Journal of Electrical and Electronics Research (IJEER), Forex, 2022, Volume 10, Issue 3, Pages 508-517
- [12]R. Mallajoshula and I. E. S. Naidu, "Novel DSOGI-based SRF controller for power quality enhancement in three-phase-grid-connected dynamic voltage restorer integrated with photovoltaic system," Electrica, 2025, vol.25, pp.1-16
- [13]Ravikanth Mallajoshula, I. E. S. Naidu, "Power quality improvement using PV fed series active power filter with enhanced Jaya optimized PI controller", International Journal of Power Electronics and Drive Systems (IJPEDS),2024, vol. 15, pp. 2198-2212,2024.
- [14]Elahi, Mir Manjur, Puan, Pratap Sekhar and Ray, Prakash Kumar. "Performance analysis of robust SRF controller based on bat optimization for PV based hybrid DSTATCOM for power quality improvement" International Journal of Emerging Electric Power Systems. 2026, <https://doi.org/10.1515/ijeeps-2025-0463>
- [15]K. P. Vineeth, P. S. Puan, S. Sahoo, and K. S. Reddy, "Performance comparison of different controller implementation in a PV fed SAPF," Gayadhar Panda, Hassan Haes Alhelou, Ritula Thakur, Book Series, Advances in Sustainability Science and Technology, Springer nature, 2022, pp. 225–238.
- [16]Pavankumar, B., Pradhan, S. Performance Analysis of Hybrid Filter Using PI and PI-Fuzzy Based UVTG Technique. In: Das, A.K., Nayak, J., Naik, B., Vimal, S., Pelusi, D. (eds) Computational Intelligence in Pattern Recognition. CIPR 2022. Lecture Notes in Networks and Systems, vol 480. Springer, Singapore.
- [17]Pravat Kumar Ray "Power Quality Improvement Using VLLMS Based Adaptive Shunt Active Filter", CPSS Transactions on power electronics and Applications, 2018, vol.3, pp.154-162
- [18]M. Kale and E. Ozdemir, "An adaptive hysteresis band current con-troller for shunt active power filter," Electric Power System Research 2025, vol. 73, pp. 113-119

[19]R. Mallajoshula and I. E. S. Naidu, "Performance Enhancement of PV fed Dynamic Voltage Restorer using UVTG and Hysteresis Voltage Controller," *2025 International Conference on Sustainable Energy Technologies and Computational Intelligence (SETCOM)*, Gandhinagar, India, 2025, pp. 1-5



© 2026 by the B Pavankumar, and Saroj Padhan.
Submitted for possible open access publication
under the terms and conditions of the Creative
Commons Attribution (CC BY) license

(<http://creativecommons.org/licenses/by/4.0/>).