

Harmonic Mitigation in Power Systems Using an ANN-Driven Shunt Active Power Filter: A Simulation-Based Study

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ABSTRACT- This paper proposal a design-based artificial neural network (ANN) control approach for a shunt active power filter (SAPF) implemented to a three-phase nonlinear load system. Harmonic variables are extracted from the load current by a Fast Fourier Transform (FFT) and provide to a feed forward ANN that generates three phase compensating current references. The ANN-SAPF is implementation in MATLAB/design under steady-state sudden load fluctuation and asymmetrical load conditions. Using the consistent harmonic result set reported in the results section the source the current total harmonic distortion (THD) is decrease from 7.82% to 2.28%, while the PCC-voltage THD reduce from 3.59% to 1.69%. The dominant 5th and 7th order current harmonics are decreased from 4.85% and 2.35% to 0.92% and 0.66%, respectively. The ANN test the stat regression coefficient is 0.999996 as well as a test MSE of 1.2×10^{-5} . The method is presented strictly as simulation validation no experimental processor in the loop hardware in the loop or monitoring real time execution claim is made. IEEE 519 is interpreted according to PCC for voltage and current distortion criteria rather than as a universal 5% current THD limit. The results refer that the integration ANN-driven SAPF provides effective harmonic compensation over the simulated operating conditions.

Keywords: Shunt Active Power Filter; Artificial Neural Network; Harmonic Mitigation; Fast Fourier Transform; Power Quality; Nonlinear Load.

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1. INTRODUCTION

In implementation power systems the growing use of nonlinear loads power electronic converters and industrial rectifiers has increased harmonic distortion in distribution grids [1]-[2]. Harmonic currents and voltages impact from ideal sinusoidal waveforms and can rising losses cause thermal stress and waveform distortion in transformers conductors' capacitors and other network components [3]-[4]. Signal addressing approach such as the Fast Fourier Transform (FFT) and wavelet analysis remain useful for harmonic feature while smart control methods provide an additional means of mapping monitoring harmonic information to compensating commands [5], [6]. Artificial neural networks (ANNs) are operation attractive because they can approximate nonlinear input output relationships from training data and can therefore be integrated with active power filters for adaptive harmonic compensation [7]-[8].

Shunt active power filters (SAPFs) are widely used to inject

compensating currents at the point of common coupling (PCC) [9], [10]. When an ANN is combined with an SAPF, harmonic features can be transformed into current-reference commands for the voltage-source inverter (VSI). However, reported ANN-based power-quality studies differ considerably in network topology, load type, harmonic content, sampling conditions, controller implementation, and validation procedure [11], [12], [13]. Consequently, numerical comparisons among studies should be interpreted as literature context rather than as direct evidence of superiority unless the methods are evaluated under equivalent conditions. In addition, IEEE 519 current-distortion requirements are PCC-dependent and are expressed using total demand distortion (TDD) and the short-circuit ratio; therefore, a universal 5% current-THD limit is not assumed in this work [14].

This paper evaluates an ANN-driven SAPF in a three-phase system feeding a nonlinear six-pulse diode rectifier with an R-L load. The study focuses on: (i) FFT-based extraction of the fundamental, 5th, and 7th current components for ANN input; (ii) ANN generation of three-phase compensating-current references; (iii) hysteresis current tracking and PI-based DC-link regulation; and (iv) simulation assessment under steady-state, load-step, and asymmetrical-load conditions. The 11th and 13th harmonics are monitored as additional spectral indicators but are not included in the ANN input vector. The paper reports the numerical results obtained from the MATLAB/Simulink model and deliberately avoids unsupported experimental, hardware-in-the-loop, real-time execution, quantitative efficiency, or cross-study superiority claims.

2. METHODOLOGY

2.1. Overall System Structure

The diagram illustrates the control system for a three-phase VSI inverter. It is divided into two main sections: the Power Circuit and the Control Circuit, separated by a dashed line.

Power Circuit:

- Three-Phase Grid Source:** Provides a 380 V, 50 Hz supply with phase voltages v_a , v_b , and v_c .
- PCC (Point of Common Coupling):** The connection point between the grid source and the inverter.
- Nonlinear Load:** A diode rectifier with an R-L load, connected to the PCC. It draws currents $i_{La}(t)$, $i_{Lb}(t)$, and $i_{Lc}(t)$.
- SAFV (Three-Phase VSI Inverter):** The inverter itself, which takes reference currents $i_a^*(t)$, $i_b^*(t)$, and $i_c^*(t)$ and outputs currents $i_a(t)$, $i_b(t)$, and $i_c(t)$. It also handles the compensation current $i_c(t)$ at the PCC.
- DC Link:** A capacitor C_{DC} with voltage V_{DC} connects the inverter to the load.

Control Circuit:

- Current Sensor:** Measures the inverter output current $i_a(t)$ at the PCC.
- FFT Harmonic Extraction:** Extracts the 5th and 7th order harmonics from the measured current, resulting in $i_{ref}(t)$.
- ANN Controller:** An Artificial Neural Network controller with an input layer, hidden layers, and an output layer. It takes $i_{ref}(t)$ as input and produces a reference current $i_a^*(t)$.
- Gate Drivers:** Convert the reference current $i_a^*(t)$ into PWM signals for the VSI inverter.
- PWM Signal Generator:** Generates the PWM signals based on the reference current $i_a^*(t)$ and a compensation current reference i_c^* .
- DC Voltage Measurement:** Monitors the DC link voltage V_{DC} .
- DC Voltage Controller:** Maintains the DC link voltage V_{DC} at a reference value V_{DC}^* by adjusting the compensation current reference i_c^* .

2.2. Power System and Nonlinear Load Modeling

$$\begin{aligned} v_a &= V_m \sin(\omega t), \\ v_b &= V_m \sin\left(\omega t - \frac{2\pi}{3}\right), \\ v_c &= V_m \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \quad (1)$$
$$v_{dc}(t) = R i_L(t) + L \left[\frac{di_L(t)}{dt} \right] \quad (2)$$
$$i_{s(t)} = \sum_{h=1}^{\infty} I_h \sin(h\omega^0 t + \varphi_h) \quad (3)$$

2.3. SAPF Configuration and DC-Link Dynamics

$$L_f \left[d \frac{i_f}{dt} \right] = v_{inv} - v_{PCC} - R_f i_f \quad (4)$$
$$C_{dc}V_{dc}\left[\frac{dV_{dc}}{dt}\right] = P_{ac} - P_{loss} \quad (5)$$

2.4. Harmonic Detection via FFT

$$X[k] = \sum_{n=0}^{N-1} x[n]w[n]\exp\left(-\frac{j2\pi kn}{N}\right) \quad (6)$$
$$x_f = [|I_1|, \angle I_1, |I_5|, \angle I_5, |I_7|, \angle I_7]^T \quad (7)$$

790

vector. This choice emphasizes the fundamental component and the two dominant characteristic harmonics while keeping the ANN input dimension small. Orthogonality of the DFT basis and Parseval's relation support spectral decomposition and energy accounting across DFT bins, but they do not prove that a selected subset of harmonics is universally comprehensive or non-redundant. Accordingly, the feature-selection claim is limited to the operating conditions evaluated in section 4.

2.5. ANN-Based Reference Current Generation

A multilayer feed-forward ANN maps the six FFT integration input features to the three-phase compensating current reference vector. As depicted in fig. 2, the ANN has a 6–20–15–3 design comprising six input neurons two hidden layers with 20 and 15 neurons respectively and three output neurons representing to the three-phase compensating-current references.

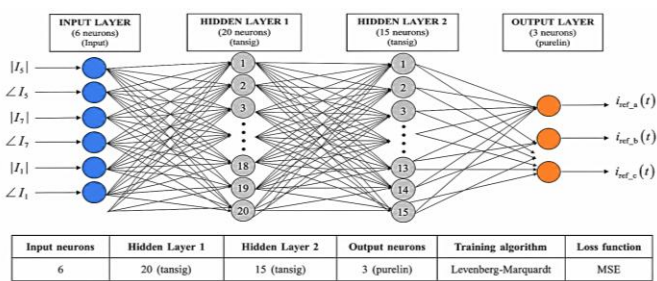


Figure 2. Structure of the feed-forward ANN (6-20-15-3).

2.5.1. Forward Propagation

For layer l with weight matrix $W(l)$, bias vector $b(l)$, and activation function $f(l)$, the neuron output is:

$$ai(l) = f(l) \left(\sum_j wij(l)aj(l-1) + bi(l) \right) \quad (8)$$

The hidden layers use the hyperbolic tangent activation function (tansig), whereas the output layer uses a linear activation (purelin) to generate continuous current-reference values.

2.5.2. Levenberg Marquardt Optimization Algorithm

This network is trained by reduce the mean squared error between the target compensating currents and the ANN outputs:

$$E(w) = \left(\frac{1}{2} \right) \sum_{p=1}^P \sum_{o=1}^O [t_{po} - a_{po}(w)]^2 \quad (9)$$

where t and a denote the target and ANN output values over the training patterns and output channels. The Levenberg-Marquardt (LM) weight update used in the training formulation is:

$$w(k+1) = w(k) - [J^T J + \mu I]^{-1} J^T e \quad (10)$$

where J is the Jacobian matrix of the error vector e with respect to the weight vector w , μ is the adaptive damping parameter, and I is the identity matrix. For small μ , the update approaches a Gauss-Newton step; for larger μ , the damping

makes the update more gradient-descent-like. These limiting behaviors motivate the LM algorithm but do not constitute a proof of global convergence or monotonic error reduction for the present nonconvex ANN training problem.

2.5.3 Training Data Generation

The ANN dataset contains 5,000 simulated operating samples generated around the nominal system point in table 1. To ensure reproducibility, the nonlinear-load resistance R is sampled from a uniform distribution over 8–12 Ω , the load inductance L from 40 - 60 mH, and the phase RMS supply voltage from 198–242 V ($\pm 10\%$ around the nominal 220 V). A fixed random seed of 42 is used for dataset generation. For every sample, the six-element FFT feature vector in eq. (7) is paired with the corresponding three-phase compensating-current target generated by the instantaneous p - q theory reference calculation. Each input feature is scaled to the interval $[-1,1]$ using minimum and maximum values computed from the training subset only; the same scaling coefficients are then applied unchanged to validation and test data. The 5,000 samples are divided into 70% training (3,500), 15% validation (750), and 15% independent holdout testing (750). The holdout test subset is excluded from weight fitting, damping-parameter adaptation, and early-stopping decisions and is evaluated only after training is completed.

Table 1. System and control parameters

Parameter	Symbol	Value
Phase voltage (RMS)	V_{rms}	220 V
Grid frequency	f	50 Hz
Load resistance	R	10 Ω
Load inductance	L	50 mH
SAPF coupling inductance	L_f	2 mH
DC-link capacitance	C_{dc}	2200 μF
DC-link reference voltage	$V_{dc,ref}$	700 V
Sampling / simulation step	T_s	5×10^{-5} s
Training samples	N_s	5,000
Data split (train/val/test)	—	70/15/15 %
Dataset R range	R_{train}	Uniform [8, 12] Ω
Dataset L range	L_{train}	Uniform [40, 60] mH
Dataset phase-voltage range	V_{train}	Uniform [198, 242] V RMS
Random seed	—	42
Hysteresis half-band	HB	0.5 A
PI proportional gain	K_p	0.8
PI integral gain	K_i	40 s ⁻¹
ANN update interval	TANN	1×10^{-4} s
FFT window length	TFFT,w	20 ms (1 cycle)
FFT refresh interval	TFFT,u	1 ms

Table 2. ANN architecture and training settings

Item	Specification
Topology	6 → 20 → 15 → 3
Input features	I5 , ∠I5, I7 , ∠I7, I1 , ∠I1
Output	3-phase compensating currents
Hidden activation	tansig (tanh)
Output activation	purelin (linear)
Training algorithm	Levenberg–Marquardt
Performance index	MSE
Achieved test R ²	0.999996
Input normalization	Min–max scaling to [−1,1] using training-subset extrema only
Data-generation ranges	R: 8–12 Ω; L: 40–60 mH; Vrms: 198–242 V; uniform distributions
Random seed	42
Data split	70/15/15% = 3500/750/750 samples
Test methodology	Independent holdout; excluded from training and early stopping

2.6. Hysteresis Current Control

A hysteresis current controller directly generates inverter switching commands from the error between the ANN reference current and the measured filter current. For the adopted simulation configuration, the hysteresis half-band is $HB = 0.5$ A. This value was selected through iterative time-domain tuning as a compromise between current-tracking ripple and switching activity. The electrical network is solved with a discrete fixed step of 5×10^{-5} s, and the hysteresis comparator is evaluated at the same rate. No separate fixed-frequency PWM block is used. The ANN reference is updated every 1×10^{-4} s, while FFT features are computed from a one-cycle (20 ms at 50 Hz) Hann-windowed record and refreshed every 1 ms. These rates explicitly separate the electrical solver, ANN update, and spectral-feature update.

For phase a, with $e_a = i^* f, a - i_f, a$, the hysteresis switching law is:

$S_a = ON$ for $e_a > +HB$; $S_a = OFF$ for $e_a < -HB$; and the previous switching state is retained for $|e_a| \leq HB$.

The hysteresis law confines the tracking error approximately within $\pm HB$ under the assumed switching model. The adopted PI gains are $K_p = 0.8$ and $K_i = 40 \text{ s}^{-1}$. They were selected by iterative simulation tuning to obtain stable DC-link regulation with limited oscillation under the nominal and load-step cases. These controller settings are reported explicitly in Table 1 to support reproducibility.

The hysteresis law provides a bounded tracking region by construction, but the resulting switching frequency varies with

the DC-link voltage, coupling inductance, grid voltage, current-reference slope, and hysteresis width. Therefore, no fixed switching-frequency value or formal stability guarantee is inferred from the hysteresis bound alone.

2.7. DC-Link Voltage Regulation

A PI controller regulates the DC-link voltage by adding the active-current component required to maintain V_{dc} near its reference:

$$i_{dc}^* = K_p(V_{dc,ref} - V_{dc}) + K_i \int (V_{dc,ref} - V_{dc}) dt \quad (12)$$

This emargin term removes steady-state offset for the idealized regulation model when the closed loop is stable and unsaturated. The simulation reference used consistently in the revised manuscript is $V_{dc,ref} = 700$ V.

2.8. Performance Metrics

The principal reported metric is source-current total harmonic distortion (THD) calculated using eq. (13), complemented by PCC-voltage THD, individual harmonic magnitudes, ANN regression performance, and robustness under load variations.

$$THD_I (\%) = 100 \times \frac{\sqrt{\sum_{h=2}^H I_h^2}}{I_1} \quad (13)$$

IEEE 519 compliance is not inferred from a universal 5% current-THD threshold. At the point of common coupling (PCC), IEEE Std 519-2022 specifies voltage-distortion limits and current-distortion limits that depend on system conditions, including the short-circuit ratio and total demand distortion (TDD) [21]. Because the present simulation does not provide the utility short-circuit current and demand-current quantities required for a rigorous I_{sc}/I_L -based TDD assessment, the study reports current THD as a power-quality performance metric rather than claiming formal current compliance. The obtained PCC-voltage THD of 1.69% is reported quantitatively, while a complete IEEE 519 current-compliance assessment is reserved for future work with explicitly specified PCC short-circuit and demand-current data.

3. SIMULATION SETUP AND EVALUATION

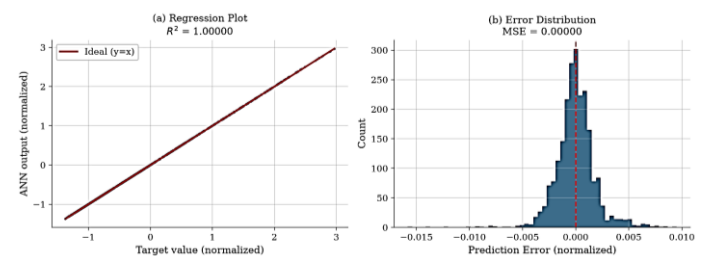


Figure 3. ANN training performance: regression plot and error distribution

Note: Values displayed inside the regression/error plots are rounded for visualization; the tabulated independent-test values are $R^2 = 0.999996$ and $MSE = 1.2 \times 10^{-5}$.

Table 3. Simulation results summary

Metric	Before SAPF	After SAPF
Current THD	7.82 %	2.28 %
Current THD reduction	—	70.8 %
Voltage THD	3.59 %	1.69 %
ANN test R ²	—	0.999996
ANN test MSE	—	1.2×10^{-5}

This system was designed in MATLAB Simulink using a discrete solver with a simulation step of $T_s = 5 \times 10^{-5}$ s. The consistent result set used throughout the manuscript is summarized in *tables 3 and 4*: source current THD reduce from 7.82% to 2.28%, and PCC voltage THD reduce from 3.59% to 1.69%. *Figure 4* is included only as a representative laboratory hardware platform for future implementation and was not used to generate the reported simulation results.

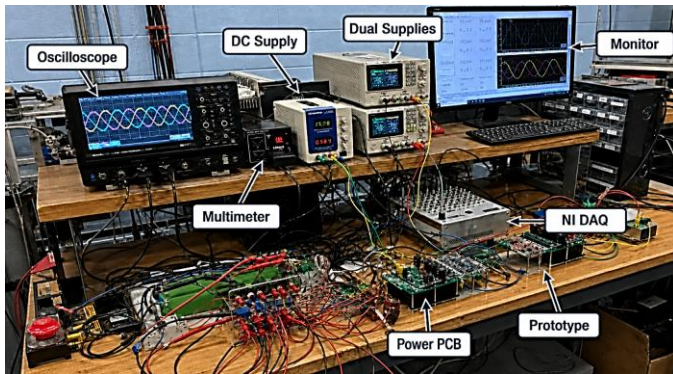


Figure 4. Representative laboratory hardware platform for future experimental implementation (illustrative only; not used to generate the simulation results reported in this paper).

4. RESULTS AND DISCUSSION

These results evaluate the ANN-SAPF under steady state transient, and asymmetrical-load conditions using the same validated numerical dataset. The discussion is limited to quantities directly supported by the MATLAB/Simulink results. No processor execution, laboratory measurement, hardware in the loop validation quantified efficiency enhancement or universal IEEE 519 current compliance claim is made.

4.1. Spectral Precision and Steady State Mitigation

Under uncompensated conditions the nonlinear R-L load provide through the three-phase diode rectifier result visibly distorted PCC waveforms. As present in *fig. 5* and the spectral results included in *table 4* the baseline source-current THD is 7.82%, with the 5th and 7th harmonics providing the dominant low-order contributions expected from a six-pulse rectifier.

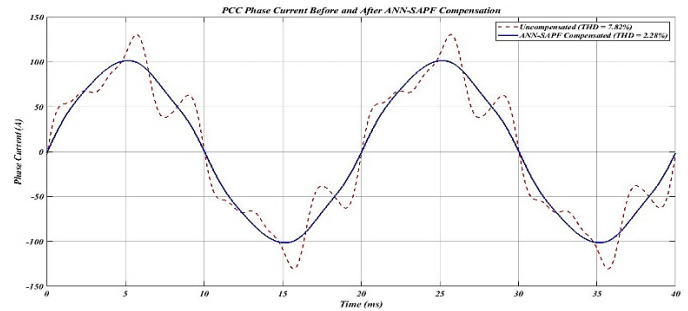


Figure 5. PCC phase-current waveforms before and after ANN-SAPF compensation

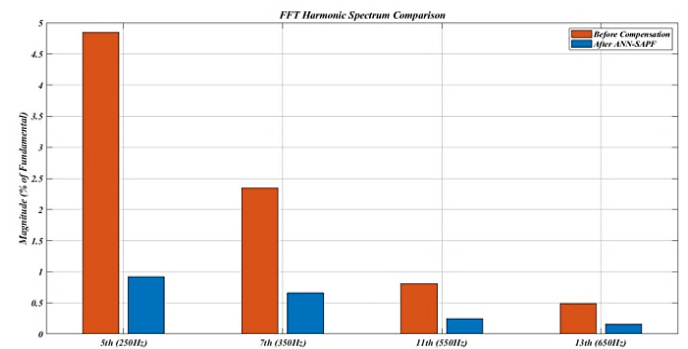


Figure 6. Harmonic-content comparison at the PCC before and after ANN-SAPF compensation

After ANN-SAPF compensation the source-current waveform becomes substantially closer to sinusoidal. *Table 4* shows that the 5th current harmonic decreases from 4.85% to 0.92%, the 7th from 2.35% to 0.66%, the 11th from 0.81% to 0.25%, and the 13th from 0.49% to 0.16%. The resulting source-current THD decreases from 7.82% to 2.28%, while the PCC-voltage THD decreases from 3.59% to 1.69%. These values are used consistently throughout the abstract, tables, results, and conclusion.

Table 4. FFT harmonic attenuation at the PCC

Harmonic Order	Current (Before)	Current (After)	Voltage (Before)	Voltage (After)
5 th (250 Hz)	4.85%	0.92%	2.25%	0.78%
7 th (350 Hz)	2.35%	0.66%	1.12%	0.52%
11 th (550 Hz)	0.81%	0.25%	0.27%	0.13%
13 th (650 Hz)	0.49%	0.16%	0.20%	0.10%
Total THD	7.82%	2.28%	3.59%	1.69%

4.2. Dynamic Transient Tracking and Power Balancing

To evaluate dynamic behavior, a 50% step increase in nonlinear-load demand is applied at $t = 5.0$ s. The source-current THD remains below 2.45% during the evaluated transient. The DC-link reference is consistently set to $V_{dc,ref} = 700$ V. Because minimum DC-link voltage and settling-time

values are not part of the retained validated result set, no numerical voltage-recovery-time claim is made.

The PI-regulated DC link is evaluated using $V_{dc,ref} = 700$ V throughout the simulation description. The transient analysis therefore focuses on the supported current-THD result rather than on an unverified setpoint-dependent recovery-time value.

4.3. Asymmetrical-Load Robustness

An asymmetrical loading profile is applied with Phase A at 150% of the nominal load, Phase B at 100%, and Phase C at 50%. Under this test, the compensated source-current THD is 2.68% (table 5). A complete quantitative current-unbalance assessment would additionally require per-phase RMS currents, negative-sequence current, current-unbalance factor, and per-phase THD. Because those quantities are not contained in the available simulation record, this case is interpreted as a robustness test for harmonic distortion under unequal phase loading rather than as a complete validation of current-unbalance compensation.

Table 5. Dynamic performance under extreme grid anomalies

Operating scenario	Current THD	DC-link settling	Interpretation
Nominal	2.28%	Not quantified	Balanced nominal case
+50% load step	2.45%	Not quantified	Stable THD tracking
150/100/50% phase loading	2.68%	Not quantified	Robust THD; unbalance metrics not available

4.4. Scope of Efficiency and Loss Claims

A quantitative system-efficiency assessment requires synchronized input- and output-power measurements together with a validated loss model for semiconductor conduction and switching, interface resistance, and magnetic components. The available simulation record does not contain the complete power and component-loss data needed for such a calculation. Therefore, this study does not infer an efficiency gain from THD reduction alone and limits its quantitative conclusions to the harmonic-mitigation and control-performance results directly supported by the simulation.

4.5. Comparative Literature Context

Table 6 places the proposed method in qualitative context with related studies already cited in the manuscript [3], [8], [9]. These works address different converter topologies control objectives, network configurations, and validation procedures. Accordingly, the comparison identifies methodological differences and does not treat separately reported numerical metrics as a head-to-head benchmark. No universal superiority, lower computational cost, or faster execution claim is made.

Table 6. Contextual comparison with related literature.

Study / method	Control / focus	Test-condition difference	Interpretation
Penthi et al. [3]	ANN-controlled 4-leg VSC-based DSTATCOM	Different converter and compensation topology	Related ANN power-quality context
Katta et al. [8]	CNN-assisted SRF control for single-phase UPQC	Single-phase UPQC with different control structure	Qualitative context only
Sapkota et al. [9]	ANN-based harmonic component prediction	Prediction task rather than closed-loop SAPF control	Qualitative context only
Proposed study	FFT-driven ANN-SAPF	Three-phase diode-rectifier load in MATLAB/Simulink	Present simulation case

5. CONCLUSION

This proposal investigated a simulation integrated ANN driven shunt active power filter for harmonic reduction in a three-phase system feeding a nonlinear R-L rectifier load. The key findings are:

1. The source-current THD declined consistently from 7.82% to 2.28%, whereas PCC-voltage THD was reduced from 3.59% to 1.69%.
2. The fifth-order current harmonic was reduced from 4.85% to 0.92% and the 7th from 2.35% to 0.66%; the 11th and 13th order additional current harmonics were suppressed.
3. During a 50% load variation test the source current THD was maintained below 2.45%. The DC side voltage reference was regulated at 700 V no unconfirmed numerical response recovery time is reported.
4. Robustness under asymmetrical loading: For the 150/100/50% phase-loading case, the compensated source-current THD was 2.68%. A complete current-unbalance assessment requires additional per-phase and negative-sequence metrics, which were not available in the retained simulation record.
5. Efficiency and loss interpretation: No numerical efficiency-gain claim is made because the available simulation record does not include a complete synchronized input/output power dataset and component-loss model. The conclusions are therefore limited to supported harmonic and dynamic-performance quantities.
6. Literature benchmarking: Related studies [3], [8], and [9] are used only to provide qualitative methodological context because they employ different converter topologies, control objectives, and validation conditions. Therefore, no numerical superiority claim is made across non-equivalent studies.

Overall, the simulation results show that the ANN-driven SAPF substantially attenuates the dominant harmonic components and maintains stable transient harmonic performance under the investigated operating scenarios.

Experimental, HIL, processor-execution, quantitative efficiency, and formal IEEE 519 current-compliance validation remain subjects for future work.

Future Work: Future work should reproduce the controller on a processor-in-the-loop or hardware-in-the-loop platform, measure execution time and switching frequency directly, provide the PCC short-circuit ratio needed for a complete IEEE 519 current-distortion assessment, and implement a detailed semiconductor and magnetic-loss model for quantitative efficiency evaluation. Additional tests should also report phase RMS currents, negative-sequence current, current-unbalance factor, and per-phase THD under asymmetrical loading.

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